제 2 장 Chemical Vapor Deposition (CVD, 화학기상증착)

1. Introduction

(1) 실리콘 소자 제조에 사용되는 박막의 종류 및 용도

분류	막의 종류		증착 기술	용도
절연막	실리콘 산화막	열산화막 (SiO_2)	Oxidation	게이트 산화막 Isolation
		CVD-SiO_2	APCVD, LPCVD	ILD, Passivation 이온 주입 Mask
		PSG	APCVD, LPCVD, PECVD	ILD, 확산 source
		BPSG	APCVD, LPCVD, PECVD	ILD
		Plasma-SiO	PECVD	ILD, Passivation
		SOG	도포법	ILD
	실리콘 질화막	Si_3N_4	LPCVD	선택산화, MNOS
		Plasma-SiN	PECVD	Passivation
반도체막	단결정 실리콘		Epitaxy	Epitaxy 층
	다결정 실리콘		LPCVD	게이트전극, 배선
금속막	Al, Mo, W, Cu, Ti $TiSi_2$, $MoSi_2$, WSi_2		Sputtering, CVD	전극, 배선

(2) PVD vs CVD 비교

- PVD (physical vapor deposition)

- 저압 chamber 내 입자의 평균자유행로(mean free path)가 chamber의 dimension보다 클 때 증착할 입자들을 열에너지 또는 Ar의 운동량 전달 등의 물리적인 힘을 가하여 박막을 증착하는 방법 (evaporation, sputtering…)

- CVD (chemical vapor deposition)

- 기체 상태에서 이종화합반응을 통하여 미세구조를 갖는 고체상태의 박막을 증착하는 방법. PVD와 같은 고진공은 필요하지 않음.
- 예제: $SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$

(3) CVD의 장·단점

- 장점

- 저온공정 (← vs. Oxidation, Nitridation…)
- 불순물의 분포와 농도를 조절가능
- 두께의 조절 가능/용이 : 수십 Å~수십 mm
- 열역학적 평형반응에 가까움
- 반응 gas의 선택이 가능
- 절연체위에도 증착 가능
- 대량 생산이 가능
- Step coverage가 좋음
- 기판을 in-situ etching 가능

- 단점

- 반응 변수가 많음
- 위험한 가스의 사용
- 장치가 복잡

2. CVD의 기본 원리

(1) CVD의 장점

- 고순도 film 형성
- 고생산성
- 공정 자동 제어 용이
- 재료의 선택에 의한 각종 film의 증착이 가능

(2) Grove Film Growth Model

□ CVD의 원리

반응 가스 ---> 고체 + 가스 부산물

$2AX(g) + H_2(g) \longrightarrow 2A(s) + 2HX(g)$

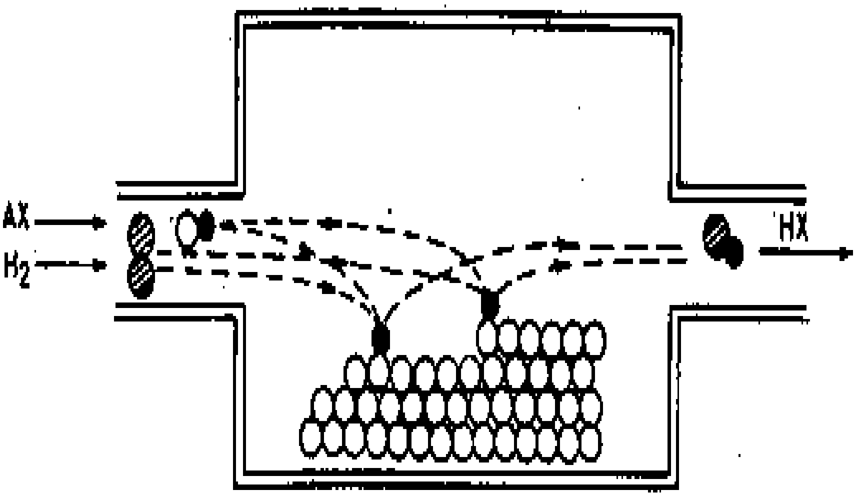
□ 막의 증착 과정

① reactor 안으로 주입된 반응 가스가 웨이퍼 표면 위로 이동

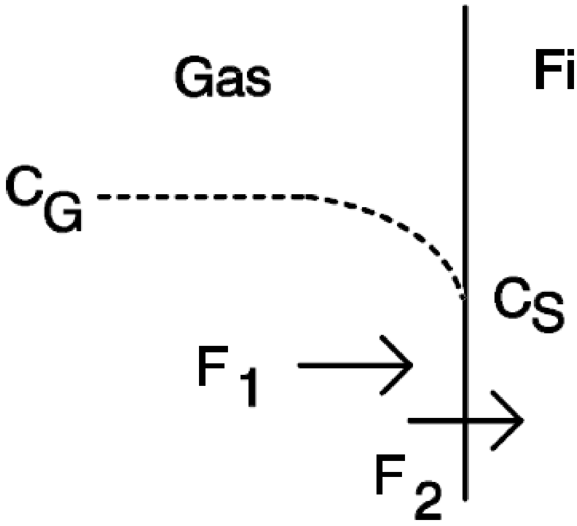
② 반응 가스가 표면에 흡착

③ 화학반응으로 웨이퍼 표면에 막을 증착하고, 반응 부산물 생성

④ 반응부산물 가스가 웨이퍼 표면으로부터 탈착하여 reactor의 gas stream으로 증발된 후 밖으로 배출



□ Film Growth Kinetics



$F_1 = h_g\ (C_g - C_s)$
$F_2 = k_s C_s$

여기서, h_g: gas-phase mass transfer coefficient
k_s: chemical surface reaction rate constant

At steady state: $F = F_1 = F_2$

$\therefore\ h_g(C_g - C_s) = k_s C_s$

$$\therefore\ C_s = \frac{h_g}{k_s + h_g} C_g$$

$$\therefore\ F = k_s C_s. = \frac{k_s h_g}{k_s + h_g} C_g$$

$$\therefore\ GR = F/\ N_1 = \frac{k_s h_g}{k_s + h_g} \frac{C_T}{N_1} Y$$

여기서, N_1: silicon atomic density(/cm^3)
Y: mole fraction of reactant gas
C_T: total # of gas molecules/cm^3

□ 막 증착 속도의 온도 의존성

Growth rate = $\frac{k_s h_g}{k_s + h_g}\frac{C_T}{N_1}Y$

① 저온 증착시: $h_g \gg k_s$, (reaction rate limited)

$\therefore\ GR \approx k_s \frac{C_T}{N_1} Y$ 여기서, $k_s = k_0 e^{-Ea/kT}$, E_a = 1.9eV

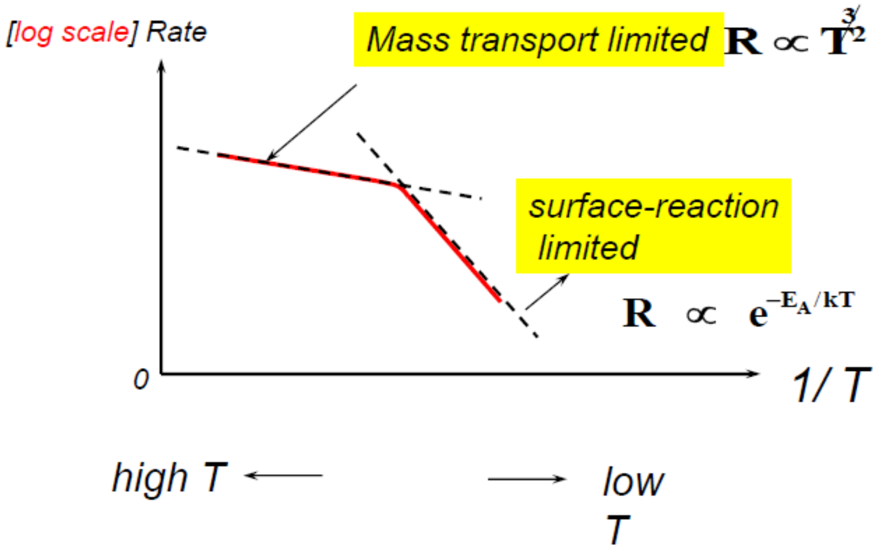
∴ 온도의 영향이 크다

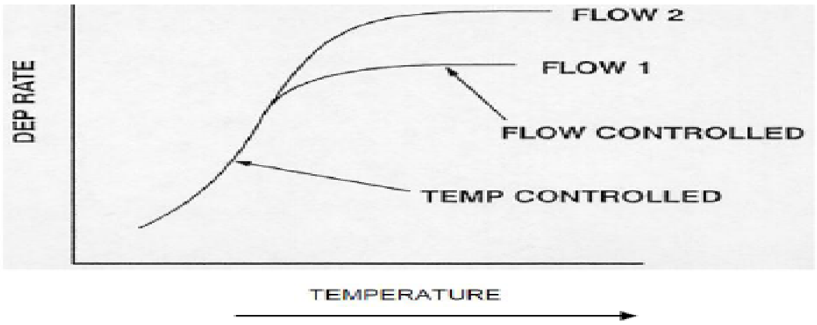
② 고온 증착시: $k_s \gg h_g$, (mass transport limited)

$\therefore\ GR \approx h_g \frac{C_T}{N_1} Y$ 여기서, $h_g \propto T^{1.5\ -\ 2.0}$

∴ 온도의 영향이 작다

Deposition Rate versus Temp





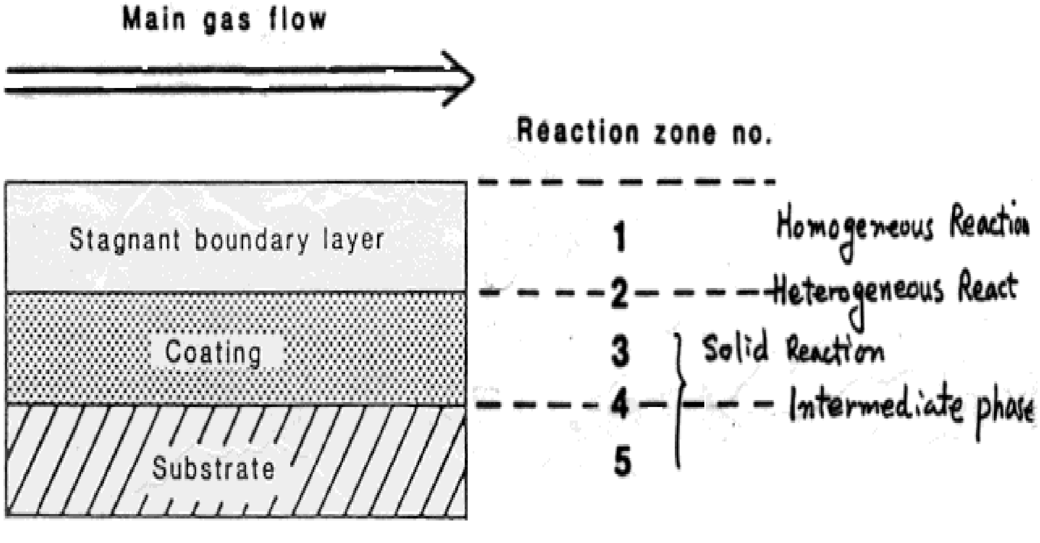
(3) Gas Phase Mass Transfer

□ Stagnant Film Model

- CVD chamber 내에서는 가스는 균일한 속도로 웨이퍼 표면 평행한 방향으로 이동: laminar flow

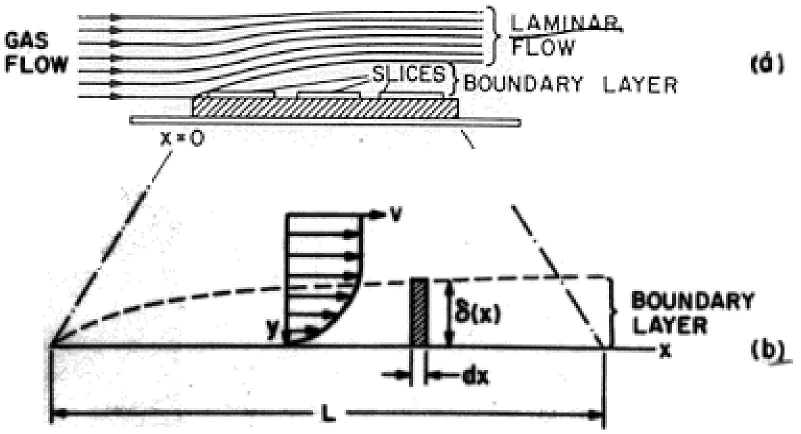
- 웨이퍼 표면에서는 가스와 웨이퍼 표면과의 마찰로 인하여 가스 flow 속도가 zero -> 웨이퍼 표면에 stagnant layer (정체층, boundary layer) 형성

- 반응 가스는 gas stream으로부터 웨이퍼 표면에 도달하기 위하여 이러한 stagnant layer를 확산에 의해 통과하여 함. 또한, gas stream과 웨이퍼 표면 사이에 반응 가스 농도와 온도가 어떤 기울기를 갖게 됨


Main gas flow
Reaction zone no.
Stagnant boundary layer
Coating
Substrate
1
2
3
4
5
Homogeneous Reaction
Heterogeneous React
Solid Reaction
Intermediate phase

Important reaction zones in CVD

□ Boundary Layer Theory


GAS FLOW
LAMINAR FLOW
SLICES
BOUNDARY LAYER
(a)
X=0
v
y
δ(x)
BOUNDARY LAYER
x
(b)
dx
L

F (friction) = $\mu\frac{dU}{dy}$ = ma

이 때, m = $\rho\,\delta$(x), a = $\frac{dU}{dt}=\frac{dU}{dx}\frac{dx}{dt}=\frac{dU}{dx}U$

∴ $\mu\frac{dU}{dy}$ = $\rho\,\delta$(x)$\frac{dU}{dx}U$ ∴ $\frac{\mu}{\rho U}dx=\delta dy$

양변을 적분하면, $\int\frac{\mu}{\rho U}dx=\int\delta dy$

∴ $\frac{\mu x}{\rho U}=\delta^2$ ∴ $\delta(x)=\sqrt{\frac{\mu x}{\rho U}}$

μ: gas viscosity, ρ: gas density
U: gas velocity at laminar flow

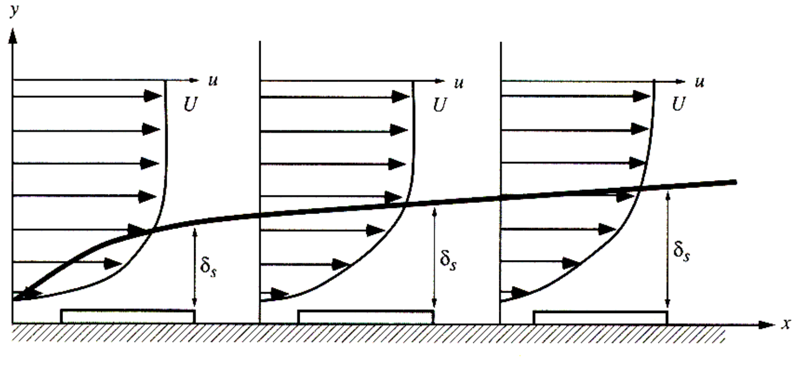

y
u
U
u
U
u
U
δ_s
δ_s
δ_s
x

Figure 9-9 Boundary layer velocities along susceptor. δ_s is the thickness of the boundary layer. The boundary layer increases with distance in the direction of the gas flow from Newton's second law. (After [9.2].)

□ Average Boundary Layer thickness

$$< \delta > = \frac{1}{L}\int_0^L \delta(x)dx = \frac{1}{L}\int_0^L \left(\frac{\mu x}{\rho U}\right)^{1/2} dx = \frac{1}{L}\frac{2}{3}\left(\frac{\mu}{\rho U}\right)^{1/2} L^{3/2}$$

$$= \frac{2}{3}\left(\frac{\mu}{\rho U}\right)^{1/2} L^{1/2} = \frac{2}{3} L\left(\frac{\mu}{\rho U L}\right)^{1/2} = \frac{2}{3}\frac{L}{\sqrt{\frac{\rho U L}{\mu}}} = \frac{2}{3}\frac{L}{\sqrt{R_e}}$$

여기서, $R_e = \frac{\rho U L}{\mu}$: Reynold number of the reactor

* When R_e is small (< 2000), gas flow is viscous. When R_e is large (>2000), gas flow is turbulent which is undesirable.

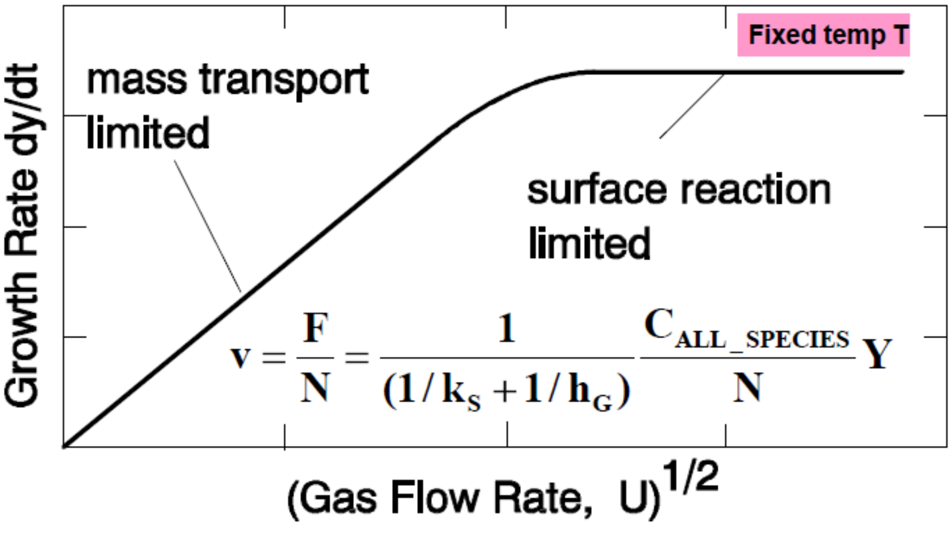
□ Growth Rate vs Flow Velocity

If growth rate is mass transport limited,

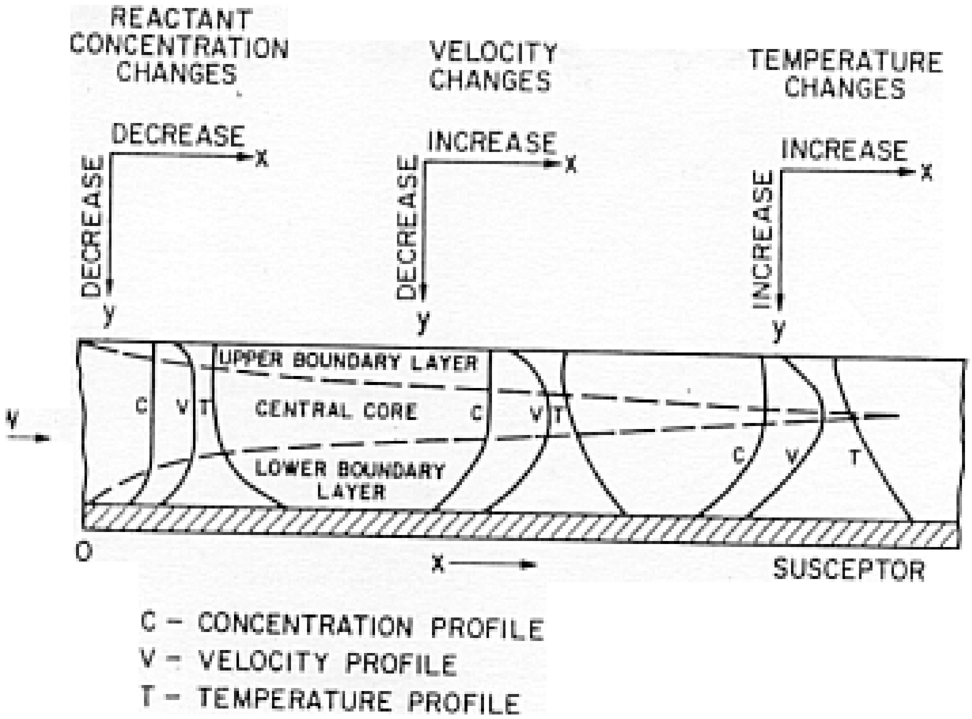
$$GR \approx h_g \frac{C_T}{N_1} Y$$

여기서, $h_g = D/\delta = \frac{D}{\frac{2}{3}\left(\frac{\mu L}{\rho U}\right)^{1/2}} = \frac{3}{2} D\left(\frac{\rho U}{\mu L}\right)^{1/2} \propto U^{1/2}$

$\therefore$ $GR \propto U^{1/2}$



□ CVD chamber 내부의 boundary layer 분포와 온도, 반응개스, 개스 유속의 분포


REACTANT CONCENTRATION CHANGES
VELOCITY CHANGES
TEMPERATURE CHANGES
DECREASE
DECREASE
INCREASE
DECREASE
INCREASE
INCREASE
x
y
UPPER BOUNDARY LAYER
CENTRAL CORE
LOWER BOUNDARY LAYER
C
V
T
v
O
x
SUSCEPTOR
C - CONCENTRATION PROFILE
V - VELOCITY PROFILE
T - TEMPERATURE PROFILE

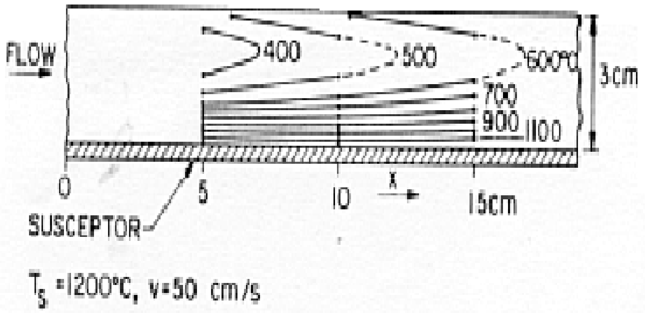

FLOW
400
500
600°C
700
900
1100
3cm
0
5
10
x
15cm
SUSCEPTOR
T_S =1200°C, v=50 cm/s

Fig. 9 Calculated temperature profiles in a horizontal reactor[4]. Reprinted with permission of the publisher, the Electrochemical Society.

(4) 핵 형성 및 박막 형성

□ Atomistic model of Epitaxial Growth

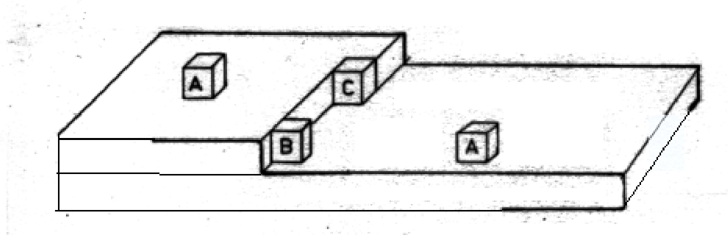


Fig. 10 Epitaxial growth model showing step-wise growth with adatoms (A), atoms on steps (B), and atoms at stable kink positions (C).

- 막의 성장은 실질적으로 수직 방향이 아니라 수평 방향으로 이루어짐. 웨이퍼 표면에 흡수된 반응 가스 분자는 급속히 확산에 의해 수평으로 이동함

□ Homogeneous Nucleation

- 반응 가스가 gas phase에서 개별적인 핵을 형성하여 웨이퍼 기판 위와 chamber 벽 등에 에피 층을 증착

- 에피 층 증착의 경우 막의 quality가 나쁨: dirty epi

□ Heterogeneous Nucleation

- 핵이 단지 웨이퍼 위에서만 형성

- 웨이퍼의 온도를 가장 높게 유지: cold-walled system

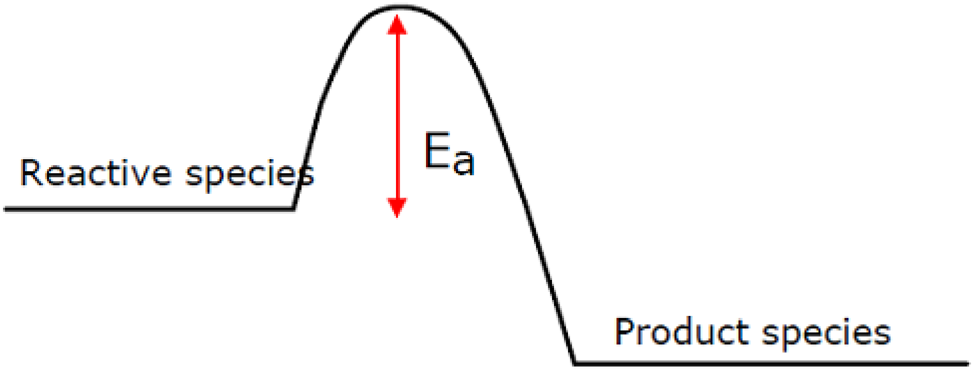
(5) CVD reaction Chemistry

- **공정 조건**

① 반응 기체와 반응 생성물의 free energy 차이가 커서 자발적인 반응이 가능해야 함

② Film은 고체, 나머지 반응 생성물의 volatile해야 함

③ Activation energy가 존재해야 함



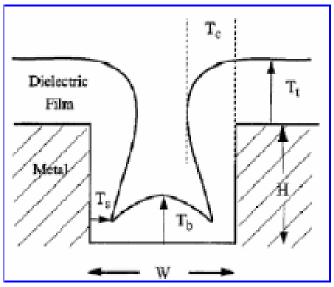
Reaction rate $R \propto \exp\left(-\frac{E_a}{kT}\right)$ → Ahrenius plot

- **Reaction type**

Type	Reaction	Example
Pyrolysis	$AB \Rightarrow A + B$	$SiH_4(g) \Rightarrow Si(s) + 2H_2(g)$
Reduction	$AX + H_2 \Leftrightarrow A + HX$	$SiCl_4(g) + 2H_2(g) \Leftrightarrow Si(s) + 4HCl(g)$
Oxidation	$AX + O_2 \Leftrightarrow AO + XO$	$SiH_4(g) + 2O_2(g) \Leftrightarrow SiO_2(s) + 2H_2O(g)$
Hydrolysis	$AX + H_2O \Rightarrow AO + HX$	$Al_2Cl_6(g) + 3CO_2(g) + 3H_2O(g)$ $\Rightarrow Al_2O_3(s) + 6HCl(g) + 3CO_2(g)$
Nitridation	$AX + NH_3 \Rightarrow AN + HX$	$3SiCiH_2 + 10NH_3$ $\Rightarrow Si_3N_4 + 6NH_4Cl + 6H_2$

(6) Step Coverage

□ 용어 정리: step coverage 란?



T_c
T_t
Dielectric Film
Metal
T_s
T_b
H
W

Aspect Ratio = H / W

Bottom step coverage = T_b / T_t

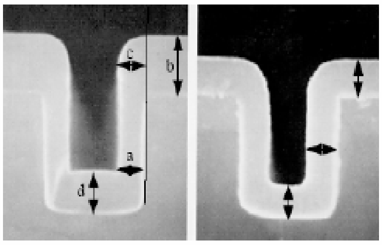
Side step coverage = T_s / T_t

Conformality = T_s / T_c

Step coverage definitions

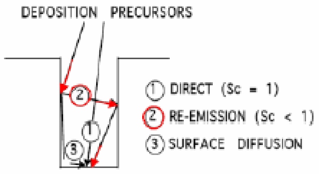
- Poor step coverage results from different deposition rates in parts of a microstructure.
- The profile of the thin film deposited by any of the CVD or PVD techniques depends upon :
  - Equipment configuration
  - Deposition method (SACVD, LPCVD, PECVD, PVD)
  - Reactant chemistry
  - Reactant transport mechanism

PETEOS vs O3 TEOS



		PETEOS	O3 TEOS
Side step coverage	= a / b	= 50%	= 95%
Bottom step coverage	= d / b	= 65%	= 95%
Conformality	= a / c	= 85%	= 99%

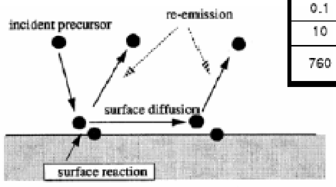
▶ Sticking Coefficient



DEPOSITION PRECURSORS
① DIRECT (Sc = 1)
② RE-EMISSION (Sc < 1)
③ SURFACE DIFFUSION

Transport of reactants to the surface at low pressure :

In most applications surface diffusion has been found to be negligible.



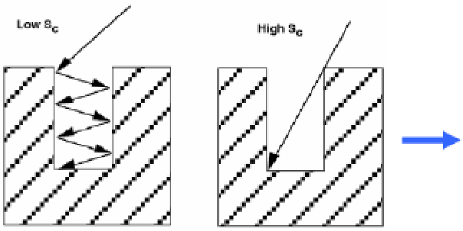
incident precursor
re-emission
surface diffusion
surface reaction

$$S_c = \frac{\Gamma_{incident} - \Gamma_{re-emission}}{\Gamma_{incident}} = \frac{\Gamma_{reaction}}{\Gamma_{incident}}$$

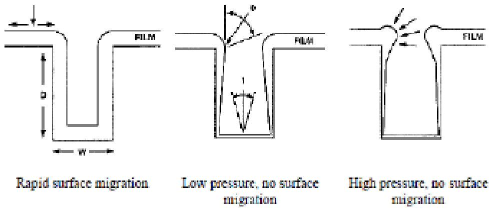
Sticking Coefficient : Sc

Reactive sticking coefficient is the probability of an incident deposition precursor...related to surface mobility.

압력 (Torr)	밀도 (분자수/㎠)	Mean free path (㎛)	flux to surface (분자수/㎠sec.)
0.1	3.2E16	500	3.8E19
10	3.2E17	50	3.8E21
760	2.5E19	0.07	2.9E23



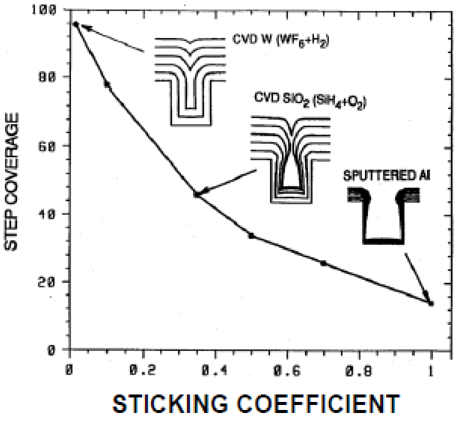
Low S_c
High S_c

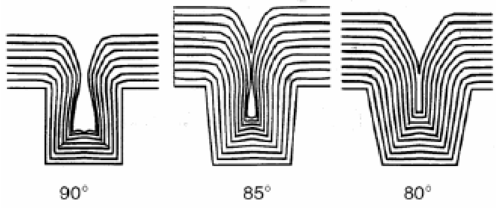


FILM
FILM
FILM
D
W

Rapid surface migration　Low pressure, no surface migration　High pressure, no surface migration

• Sticking Coefficient



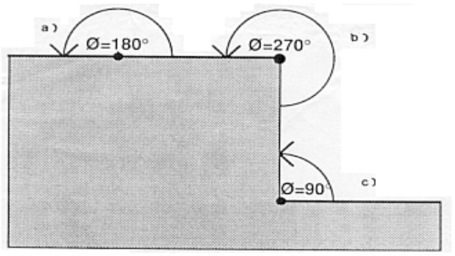


Time evolution of the profile

- Step coverage can also be improved by changing the slope of the walls.
- But this may result in an area penalty.
- Different lines show time evolution of the profile as simulated by the deposition and etch simulator SPEEDIE.

Material	Source	Temperature °C	Sc
PSG	SiH4 / O2 / PH3	400	0.35
SiO2	SiH4 / O2	400	0.26
SiO2	TEOS / O2	700	0.04
Poly-Si	SiH4	620 - 900	< 0.01
W	WF6 / H2	350 - 500	< 0.01

□ Effects of arrival angle on step coverage



□ Step coverage를 결정하는 요소

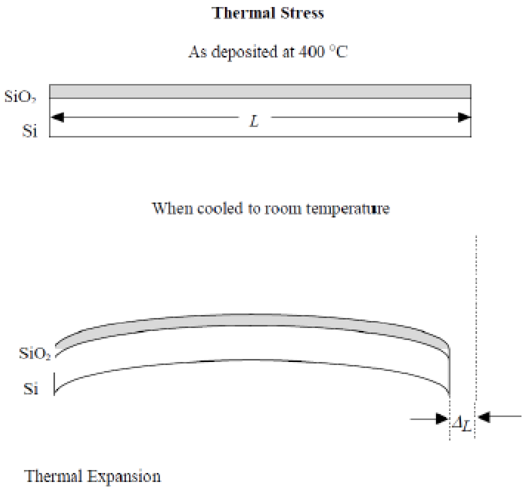
① Surface migration

- 온도의 함수. 500℃ 이상이면 conformal film 형성
- PECVD는 APCVD 보다 surface migraion이 더 활발

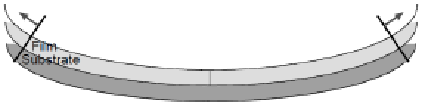
② 반응 가스의 mean free path (λ) : $\lambda = \frac{1}{\sqrt{2}} \frac{kT}{P \pi \alpha^2}$

- LPCVD, PECVD: λ= 10-100μm.
  Gas arrival은 unisotropic: shadow effect
- APCVD: λ = 0.01-0.1μm.
  Gas arrival은 isotropic: 막의 두께는 arrival angle에 비례

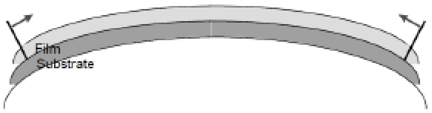
(7) Film Stress


Thermal Stress
As deposited at 400 °C
SiO₂
Si
L
When cooled to room temperature
SiO₂
Si
ΔL
Thermal Expansion

$\Delta L = \alpha \Delta T L$


Film
Substrate

Tensile Stress (+)


Film
Substrate

Compressive Stress (-)

$\alpha(SiO_2) = 0.5$*

$\alpha(Si) = 2.5$

$\alpha(Si_3N_4) = 2.8$

$\alpha(W) = 4.5$

$\alpha(Al) = 22$

* all units are in 10^{-6} °C^{-1}

- Stress Measurement

$$\sigma = \frac{E}{1-\nu}\frac{h^2}{6t}\left(\frac{1}{R_2}-\frac{1}{R_1}\right)$$

σ : stress (Pa)

E : Young's Modulus of the substrate (Pa)

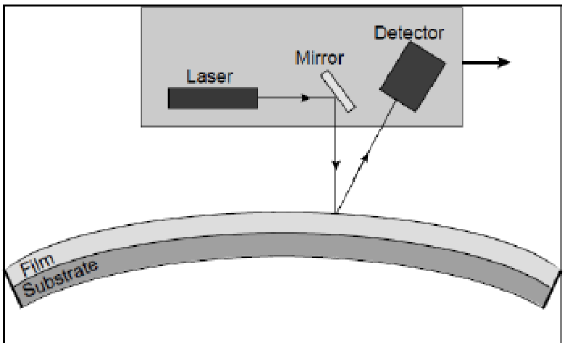
ν : Poisson's Ratio of the substrate

h : substrate thickness (μm)

t : film thickness (μm)

R_1: radius of curvature before deposition (μm)

R_2: radius of curvature after deposition (μm)


Detector
Mirror
Laser
Film
Substrate

"Cantilever Beam Technique"
Calculates the radius of curvature

3. CVD System

(1) CVD 시스템의 분류

□ reactor 내의 압력

분류		조건
APCVD	atmospheric pressure	상압 (1기압, 760 Torr)
LPCVD PECVD	low pressure	수십 Torr – 수 m Torr

□ 반응의 에너지 소스

분류		조건
Thermal CVD	저항 coil type	저항을 이용하여 susceptor를 가열
	lamp type	lamp을 이용하여 susceptor를 가열
Plasma CVD	plasma enhanced	RF 플라즈마에서 가스를 활성화함
	high density	RF로 가스를 활성화, bias로 physical etching

□ 증착되는 막의 종류에 따라서

분류		역할
Oxide CVD	SiO_2	gap fill, 절연막
	SiON	ARL, etch stopping layer
Nitride CVD	SiN	protection layer
Metal CVD	W, Ti, TiN, Cu	좋은 step coverage의 metal

□ 웨이퍼의 heating 방식

- Hot wall (radiant heating)
- Cold wall (rf induction heating)

(2) 실리콘 소자 제조에 사용되는 CVD 시스템

□ APCVD (atmospheric pressure CVD)

- 일반적인 동작 특성

- 압력: 760 torr

- 동작온도: 400 - 500 ℃

- 증착속도: mass transport limited => 웨이퍼를 수평으로 뉘어 loading => 저생산성, 많은 particle 오염

- 장점

- reactor 구조 단순 (진공펌프, rf 발생기 불필요)

- 증착 속도가 큼

- 저온 증착

- 단점

- poor step coverage

- large particle contamination

- large gas consumption

- need frequent cleaning

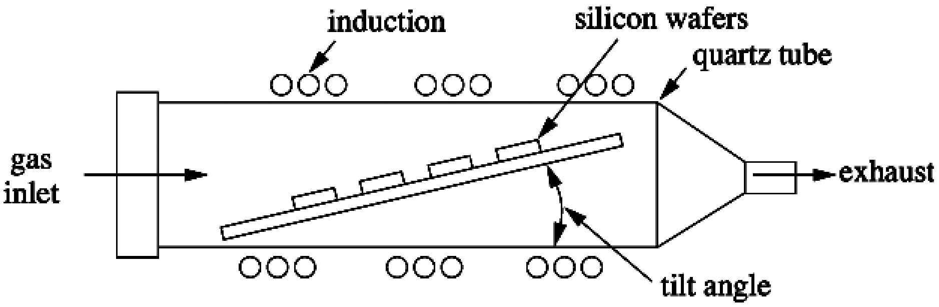
- 주 응용 분야

박막의 종류	Reaction Gas	온도 (℃)	증착속도 (nm/min)	생산성 (wafer/hr)	용도
Epitaxial Si	$SiCl_4$, H_2	1125-1120	500-1500	-	에피층
	$SiHCl_3$, H_2	1100-1150	500-1500	-	에피층
	SiH_2Cl_2, H_2	1050-1100	500-1000	-	에피층
	SiH_4,H_2	1000-1075	100-300	-	에피층
Si_3N_4	SiH_4, NH_3	900-1000	20	40	내산화막 (LOCOS)
UDO	SiH_4,O_2	450-500	100	160	ILD
	TEOS,O_2	400	-	-	sidewall spacing
PSG	SiH_4,O_2,PH_3	370-400	-	-	passivation
BPSG	SiH_4,O_2,PH_3 B_2H_6	400-450	-	-	ILD

* TEOS: $Si(OC_2H_5)_4$

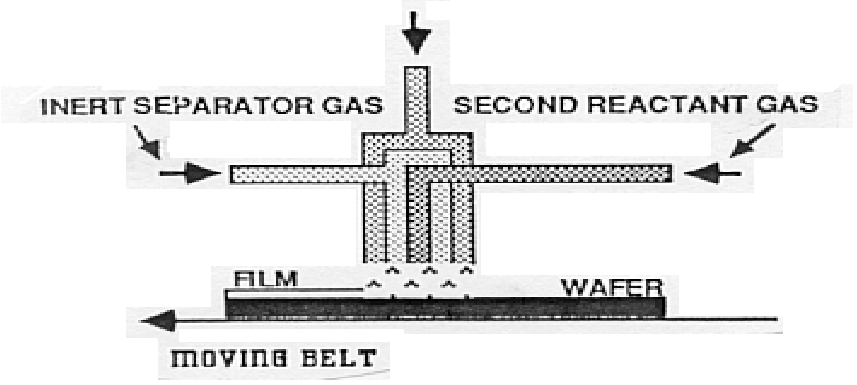
- **Reactors**

① **Horizontal tube reactor: 두께 균일성 나쁨, 생산성 낮음**


induction
silicon wafers
quartz tube
gas inlet
exhaust
tilt angle

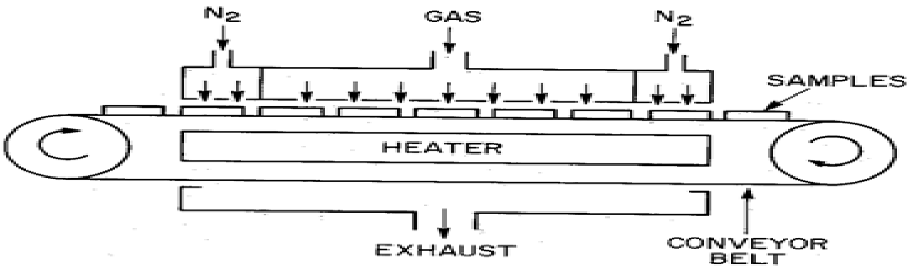
② **Gas injector type continuous processing reactor**

- Cooled nitrogen shrouded nozzle 로부터 가스 주입
- 반응가스가 수 mm 위에서 혼합 => gas phase reaction 감소
- 두께 균일성 양호, 생산성 양호, 파티클 오염 감소


INERT SEPARATOR GAS
SECOND REACTANT GAS
FILM
WAFER
moving BELT

③ **Plenum-type continuous processing reactor**

- 대기압보다 약간 높은 압력의 plenum 안에서 반응 가스 혼합
- 두께 균일성 양호, 생산성 양호, 파티클 오염 감소


N2
GAS
N2
SAMPLES
HEATER
EXHAUST
CONVEYOR BELT

□ LPCVD (low pressure CVD)

- **일반적인 동작 특성**

- 압력: 0.1 - 10 torr
- 동작 온도: 400 - 900 ℃
- 증착 속도: reaction rate limited

  ∴ 증착 속도는 온도에 아주 민감

- **Why reaction rate limited?**

- 압력이 약 1,000배 감소 (즉 1 기압 ->1 Torr)

- 가스 유속(flow velocity)가 진공 펌프로 인하여 100배 증가

- $h_g = \frac{D}{\delta}$에서

  $D \propto \frac{1}{P}$ 임으로 D는 1,000배 증가

  $< \delta > = \frac{2}{3}\left(\frac{\mu L}{\rho U}\right)^{1/2}$이고,

  $\rho(\propto P)$는 1,000배 감소, U는 100배 증가임으로

  $\langle \delta \rangle$는 약 3배 증가 (∵ $\sqrt{\frac{1,000}{100}} \approx 3$)

  ∴ h_g는 약 300배 증가 (∵ $\frac{1,000}{3} \approx 3$)

  ∴ LPCVD는 reaction rate limited !!

* 참고로 Growth rate = $\frac{k_s h_g}{k_s + h_g} \frac{C_T}{N_1} Y$

- **장점**

- excellent purity/ uniformity
- conformal step coverage (고온/ atomic gas flow)
- low pin-hole density
- large wafer capacity (vertical wafer loading)
- Less dependence on gas flow dynamics
- 낮은 파티클 오염 (due to low gas phase reaction)

- 단점
  - 낮은 증착 속도 (APCVD의 1/5 - 1/3 정도)
  - 고온 증착
  - 진공 펌프 오일 오염

- 주 응용 분야

Films		Reaction	Temp.(℃)
Si	Undoped Si	$SiH_4 \rightarrow Si + 2H_2$	580~650
	Doped Si	$SiH_4 + PH_3 \rightarrow$ P-doped Si + H_2	500~550
SiO_2	HTO	$SiCl_2H_2 + N_2O \rightarrow SiO_2 + N_2 + HCl$	820~940
	HTO, MTO	$SiH_4 + N_2O \rightarrow SiO_2 + N_2 + H_2O$	720~780
	MTO	$Si(OC_2H_5)_4 + O_2 \rightarrow SiO_2 + CO_2 + H_2O$	680~720
	LTO	$SiH_4 + O_2 \rightarrow SiO_2 + H_2O$	400~450
Si_3N_4		$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$	700~900
		$3SiCl_2H_2 + 4NH_3 \rightarrow Si_3N_4 + 6HCl + 6H_2$	650~700

- Reactors

① **End feed horizontal tube reactor**: hot wall

- Depletion effect를 줄이기 위해 tube 안쪽으로 가면서 점차 온도를 높게 함 (by 25-40℃).

- Tube 내의 온도 차로 인하여 위치에 따라 박막의 특성에 차이가 날 수 있음. 특별히 polysilicon과 doped oxide의 저온 증착(~400℃)에서 문제가 됨. 따라서 이러한 시스템은 silicon nitride나 oxynitride의 고온 증착(800-850℃) 또는 undoped polysilicon의 증착(~600℃에 사용된다.

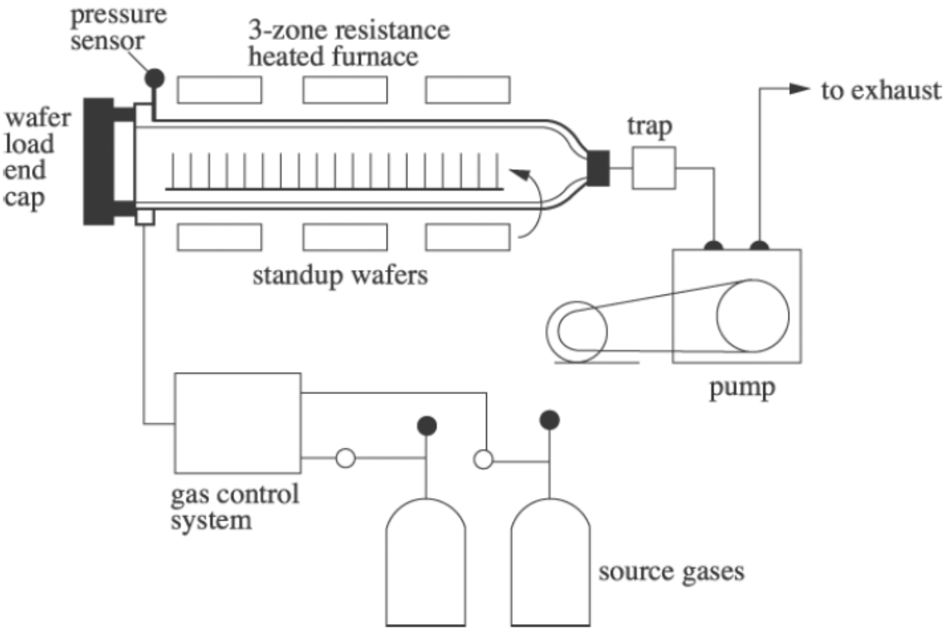
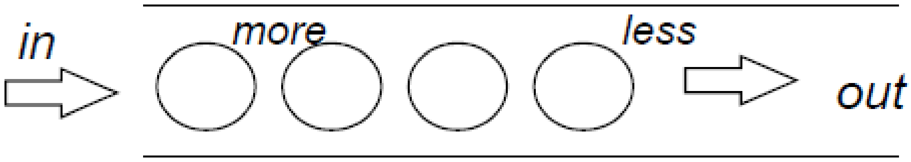

pressure sensor
3-zone resistance heated furnace
to exhaust
wafer load end cap
trap
standup wafers
pump
gas control system
source gases

Fig 3-1 LPCVD system

- Mass depletion effect



- **Solutions for mass depletion problem**

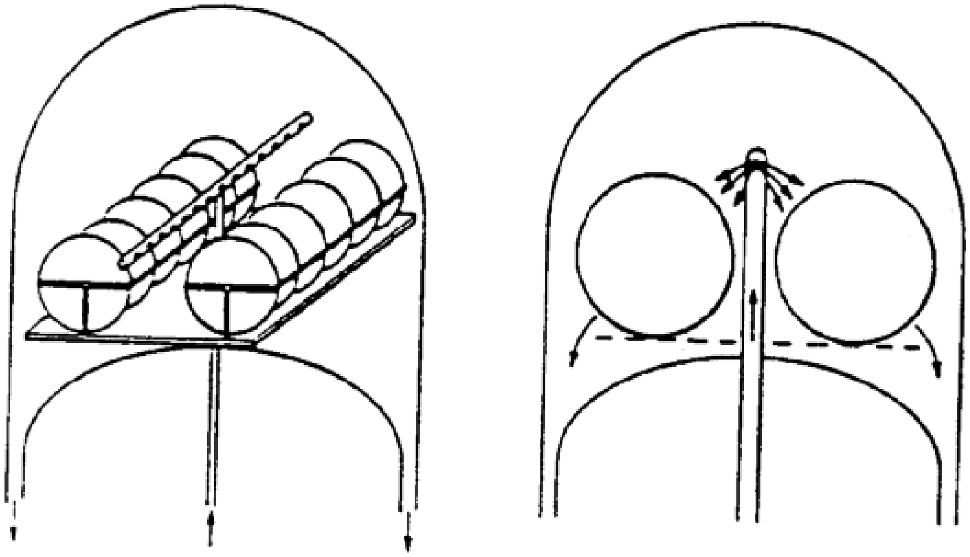
(i) Temperature ramping along reactor length

- For reaction rate limited regime

$R(x) = A \exp[-E_a/kT] \times C(x)$ where $C(x) = SiH_4$ Conc.

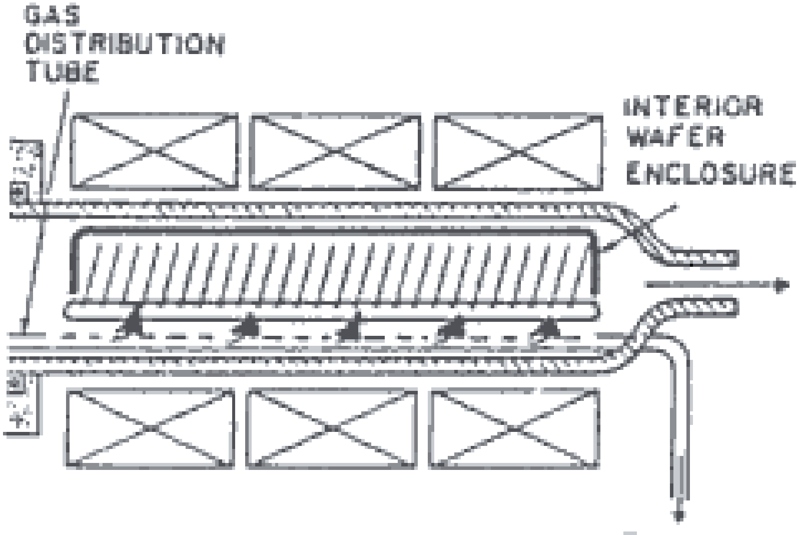
=> Creating a temperature gradient of 20 – 40° C along the tube will give better uniformity.

(ii) Distributed Feed Reactors

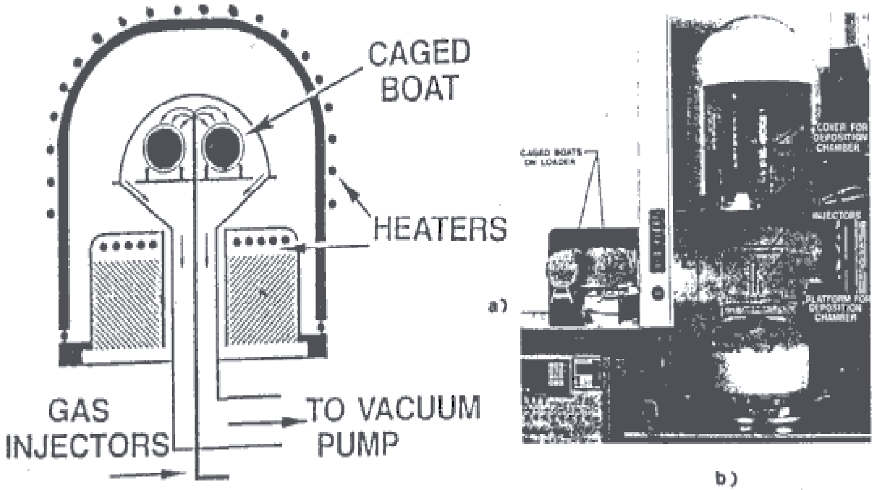


② **Distributed feed horizontal reactor(횡형)**: **hot wall**

- 가스 분할 공급 시스템: depletion effect 제거
- Tube를 따라 온도가 일정하다.
- 주로, SiO_2, PSG, BPSG의 저온증착(<600℃)에 사용됨


GAS
DISTRIBUTION
TUBE
INTERIOR
WAFER
ENCLOSURE

③ Vertical flow isothermal reactor(종형): cold wall
- 가스 분할 공급 시스템: depletion effect 완전 제거
- 낮은 파티클 오염

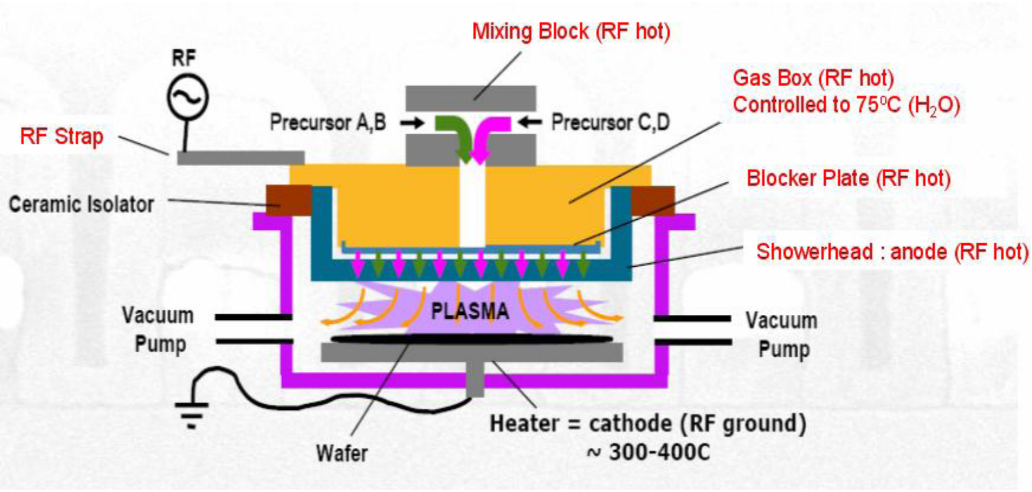

CAGED
BOAT
HEATERS
GAS
INJECTORS
TO VACUUM
PUMP
a)
CAGED BOATS ON LOADER
COVER FOR DEPOSITION CHAMBER
INJECTORS
PLATFORM FOR DEPOSITION CHAMBER
b)

Vertical isothermal LPCVD reactor. (a) Schematic drawing. (b) Photograph of system.

□ PECVD (plasma-enhanced CVD)

- 일반적인 동작 특성

- 압력: 0.1 – 5.0 torr
- 동작 온도: 200 – 500 ℃
- rf frequency: 13.56 MHz
- 증착 속도: reaction rate limited


Mixing Block (RF hot)
RF
Gas Box (RF hot)
Controlled to 75°C (H2O)
RF Strap
Precursor A,B
Precursor C,D
Ceramic Isolator
Blocker Plate (RF hot)
Showerhead : anode (RF hot)
Vacuum Pump
PLASMA
Vacuum Pump
Heater = cathode (RF ground)
~ 300-400C
Wafer

- 장점

① low temperature

– 저압상태에서 (< 수 Torr) Gas 주입, 반응 에너지로 플라즈마를 이용 – 플라즈마 에너지를 이용하기 때문에 낮은 온도에서도 증착 가능

film	precursors	Thermal deposition	Plasma-enhanced
Silicon nitride	SiH4 or SiH2Cl2 and NH3	750 C	200-500 C
Silicon dioxide	SiH4 and O2 [or often N2O]	350-550 C	200-400 C
	TEOS and O2	700-900 C	300-500 C
Amorphous silicon	SiH4	550-650 C	200-400 C

② 다양한 공정 변수가 있어 두께, stress, moisture

resistance, density control 가능
- Energetic ion bombardment (이온의 운동에너지: 수 eV ~ 수백 eV)가 증착되는 막의 특성에 심각한 영향을 줌. Ion bombardment가 증가하면 막의 밀도가 증가하고 막의 스트레스가 더 compressive 로 바뀜. 물론 지나친 compressive stress는 심각한 막의 신뢰성 문제를 야기할 수 있음. 공정조건, chamber geometry, or excitation의 변화를 통한 스트레스를 조절하고, 이를 통하여 막의 특성을 조절할 수 있음.

③ High throughput
④ Good Mechanical strength
⑤ Moisture blocking

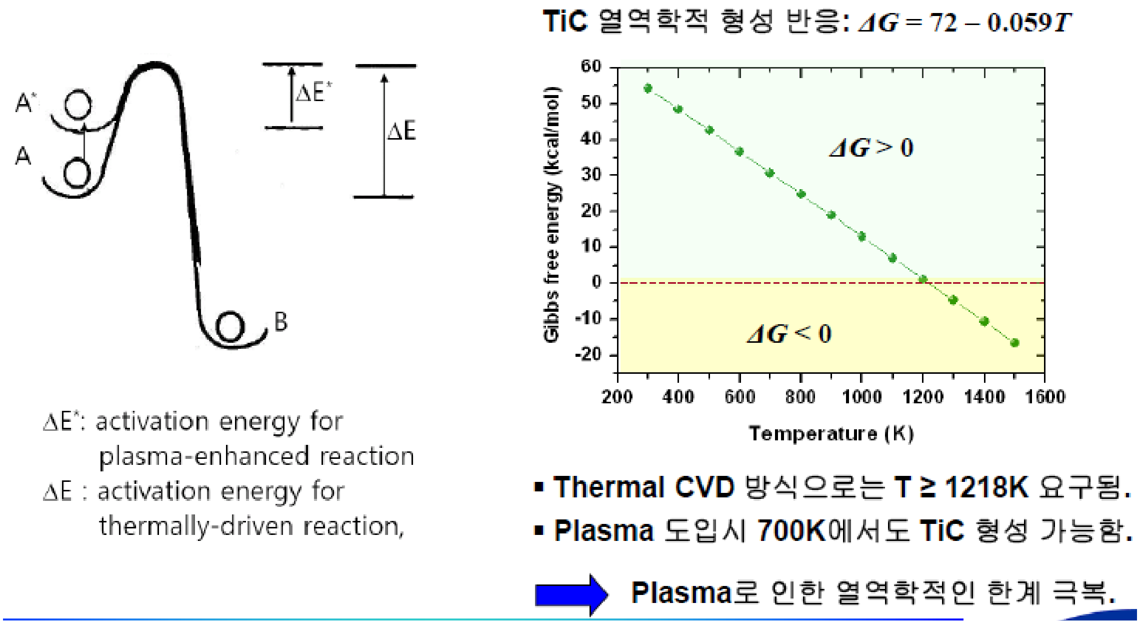
⑥ Reactor의 청소가 용이
- 예를 들면 CF_4 개스를 사용하여 plasma를 발생시키면 전극과 chamber 벽에 붙어있는 silicon, silicon nitride, or silicon dioxide를 쉽게 제거할 수 있음

- 단점

① Poor gap fill capability
② Plasma damage
③ Chemical (H_2, N_2, O_2) and particle contamination
④ Complex equipment

- 기본 개념

- 플라즈마 인가를 통한 반응에 필요한 activation energy를 감소시켜 낮은 온도에서도 성막 형성이 가능하게 함



TiC 열역학적 형성 반응: $\Delta G = 72 - 0.059T$

ΔE*: activation energy for plasma-enhanced reaction

ΔE : activation energy for thermally-driven reaction,

- **Thermal CVD 방식으로는 T ≥ 1218K 요구됨.**
- **Plasma 도입시 700K에서도 TiC 형성 가능함.**

➡ **Plasma로 인한 열역학적인 한계 극복.**

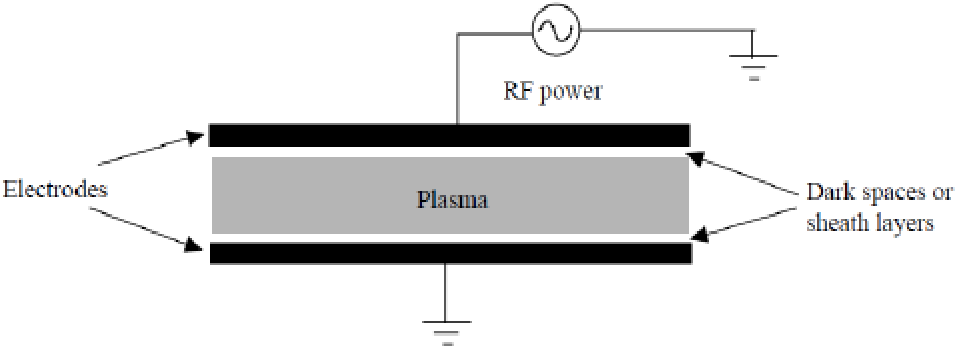
- Plasma Sequence

① RF power on the electrodes ➔ E-field

② Free e- accelerated by the field

③ High E e- → atoms and molecules ➔ ionization + more e-

④ chamber fills with e- and ions ➔ Plasma stabilization


RF power
Electrodes
Plasma
Dark spaces or sheath layers

- 플라즈마내 주요 반응

- 전자 충돌에 의한 chemical reactivity 높은 ion/radical의 형성으로 저온 반응 가능

① Ionization: $A + e^- \rightarrow A^+ + e^- + e^-$

- 전자 충돌에 의한 원자/분자로부터의 전자 탈착으로 이온 생성

- 플라즈마 상태를 지속적으로 유지하기 위한 필수적인 반응

② Excitation: $A + e^- \rightarrow A^* + e^-$

- 전자충돌에 의해 기저 상태의 원자/분자들이 여기 상태로 전이

- 다시 여기상태에서 기저상태로 전이 -> 다양한 파장의 빛 방출

- 기저 상태로 전이되지 않는 준안정 상태의 원자/분자들이 CVD 반응에 참여

③ Dissociation: $A_2 + e^- \rightarrow A^* + A^* + e^-$

- 전자 충돌에 의해 분자들이 원자 형태로 해리됨

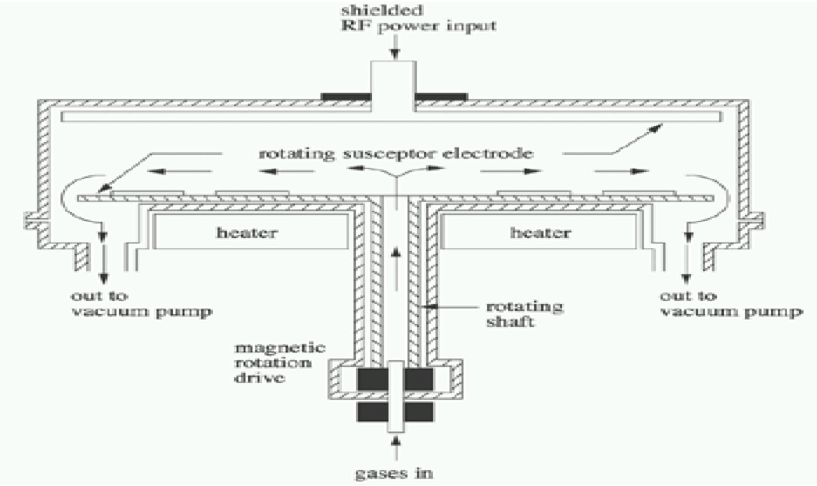
- 열역학적으로 분해가 어려운 분자들도 쉽게 해리되어 전반적인 CVD 반응이 용이해짐

- 주 응용 분야

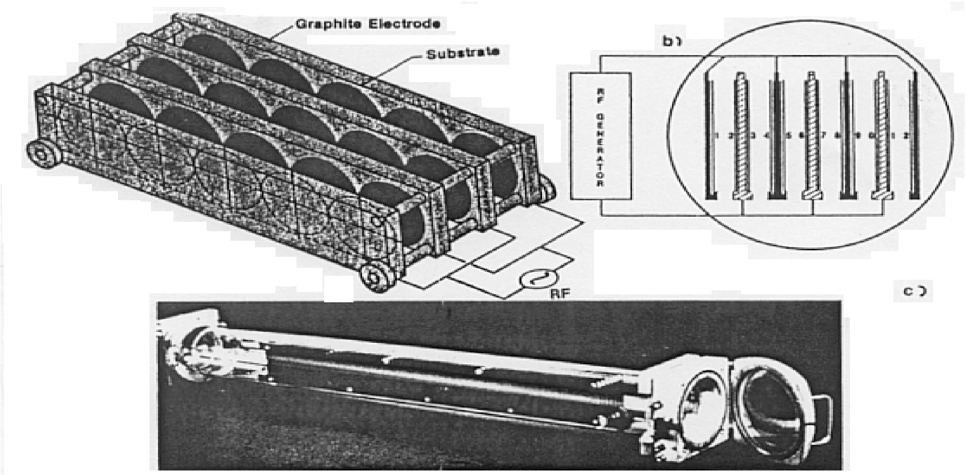
박막의 종류	Reaction Gas (Carrier)	온도 (℃)	용도
SiN	SiH_4, NH_3	250-300	passivation
	SiH_2Cl_2, NH_3	250-300	passivation
SiO	TEOS, O_2/O_3	380-400	ILD
	SiH_4, N_2O	380-400	ILD
PSG	SiH_4, N_2O, PH_3	380-400	passivation
BPSG	SiH_4, O_2, PH_3, B_2H_6	380-400	ILD

- Reactors

① **Parallel plate reactor**: cold wall
- 플라즈마 밀도와 가스 주입량의 조절에 의해 depletion 효과 감소
- reactor 벽과 전극으로부터의 particle 오염 가능
- low throughput


shielded
RF power input
rotating susceptor electrode
heater
heater
out to
vacuum pump
rotating
shaft
out to
vacuum pump
magnetic
rotation
drive
gases in

② **Horizontal tube reactor**: hot wall
- 온도 ramping과 pulsed plasma 형성에 의해 depletion 효과 최소화
- low particle 오염
- large throughput


Graphite Electrode
Substrate
b)
RF GENERATOR
RF
c)

□ CVD 시스템 특성의 상호 비교

Process	Merits	Demerits	Application
LPCVD	- Excellent uniformity - High film quality (purity) - Conformal step coverage - Large wafer capacity - Low contamination	- High temperature - Low depo. rate	- Mask, spacer (HTO, SiN) - Gate, B/L, Capacitor 전극 (Poly-Si, W, WSi) - Capacitor dielectric (TaO)
APCVD	- Simple reactor - Easy process & low cost - Fast deposition - Low temperature	- Poor step coverage - Particle generation - lots of carrier gas	- ILD (BPSG, PSG)
PECVD	- Low temperature - Fast deposition - Good step coverage	- Chemical & particle contamination - Crack & lifting - Plasma damage	- PMD - Passivation SiN

□ 박막 증착 System들 간의 특성 비교

	APCVD	LPCVD	PECVD	PVD	ALD	SOD
증착 온도 (℃)	370 – 500	400 – 900	200 – 500	상온 – 300	100 – 600	400 – 450
압력 (Torr)	760	0.1–10	0.2–5.0	0.1–1.0	0.5–1.5	760
Fine THK Control	good	good	bad	bad	excellent	good
Step Coverage	bad	very good	bad	bad	excellent	excellent
Throughput	low	low	high	high	very low	high
Pin Hole Density	not bad	not bad	not bad	high	low	high
Film	Si SiO_2 SiN PSG BPSG	Si SiO_2 SiN PSG BPSG W WSi_x	SiO_2 SiN SiC SiOC α–C	Ti TiN Al Cu TaN W	SiN TiN Al_2O_3 TaO HfO	SiO_2 SiOC α–C:H

4. 다결정실리콘 막의 증착 및 특성

(1) Polysilicon 박막의 특성

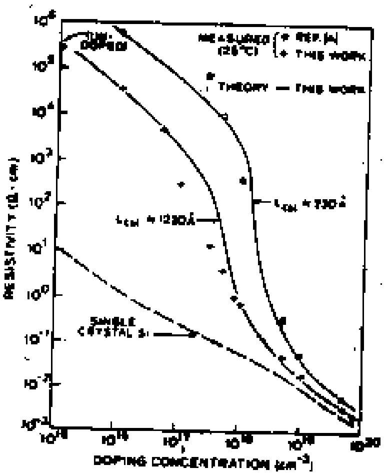
□ 물리적, 기계적 특성

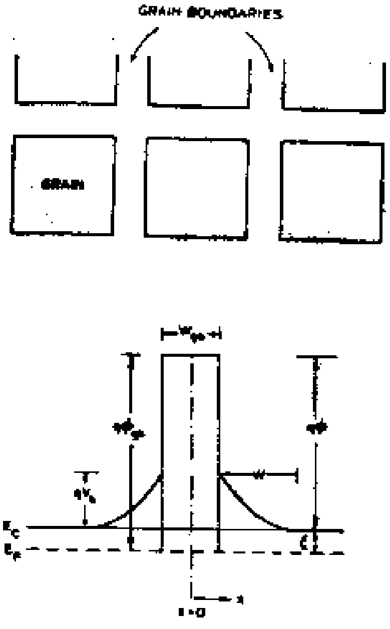
- As-deposited films:
  - 증착 온도 < 560 ° C : amorphous
  - 증착 온도 > 580 ° C : polycrystalline

- 불순물 확산계수가 grain boundary에서 100-1000배 증가
  - 불순물의 grain boundary로의 segregation:
    As, P; 大, B: 小

□ 전기적인 특성

- 농도가 낮을 때는 단결정 실리콘보다 저항이 월등히 높으나, 농도가 높아짐에 따라 점차 저항이 단결정 실리콘의 저항에 접근





GRAIN BOUNDARIES
GRAIN
W_{gb}
$q\Phi_{gb}$
$q\Phi$
qV_B
W
E_C
E_F
ξ
x
x=0

(2) CVD of Polysilicon: commonly use LPCVD

□ Reaction

$SiH_4\,(g) = Si(s) + 2H_2(g)$

□ Polysilicon 박막 생성 속도의 온도 의존성

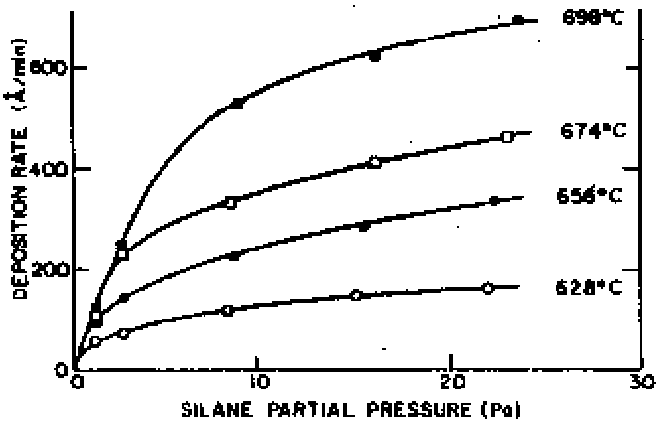


Fig. 12 The effect of silane concentration on the polysilicon deposition rate

□ 증착 속도와 불순물 농도

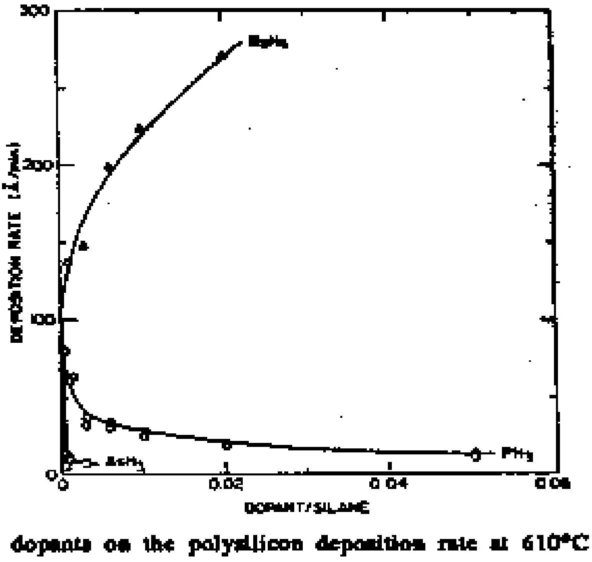


Fig. 13 The effect of dopants on the polysilicon deposition rate at 610°C

□ Polysilicon 박막의 grain 크기

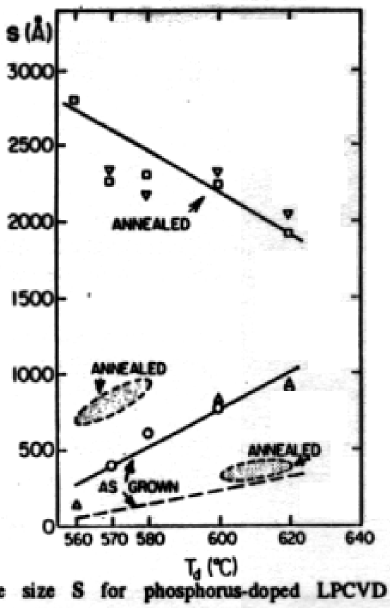
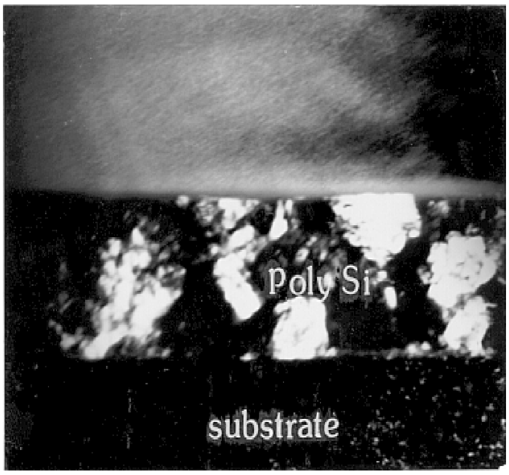


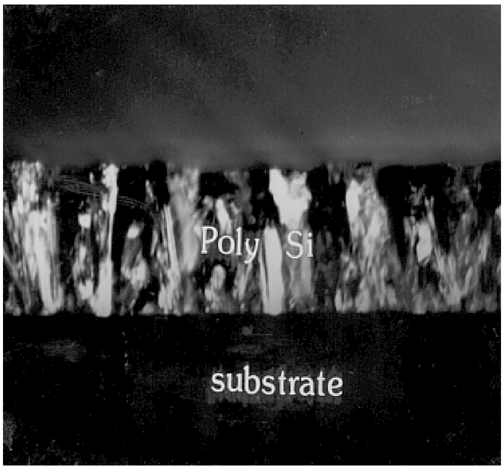
Fig. 15 Average crystallite size S for phosphorus-doped LPCVD silicon layers as-grown (o = interface, Δ = surface), and annealed at 1000°C (◊ = interface, ∇ = surface) as a function of deposition temperature, T_d. Undoped layers (dashed lines) are shown for comparison.

□ 증착 조건에 따른 Polysilicon 막의 결정 구조

- As-deposited amorphous silicon 박막의 열처리 후의 dark-field TEM micrograph



- As-deposited polysilicon 박막의 열처리 후의 dark-field TEM micrograph



(3) Doping of Polysilicon

□ 확산 (Ex: $POCl_3$ doping)

- 낮은 저항
- 고온: 800 - 900 ℃
- 표면거칠기 증가

□ 이온 주입 & anneal

- 정밀한 농도 제어 가능
- 상대적으로 높은 저항 (확산보다 약 10배)

□ in-situ doping

- 도핑 공정을 단순화시킬 수 있음
- 증착속도 및 doping uniformity 제어가 어려움

(4) Polysilicon Oxidation

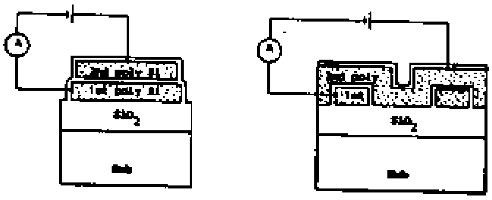


Fig.1 Measurement patterns.

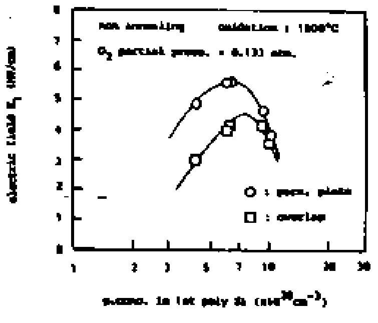


Fig.3 The relationship between the phosphorus concentration in 1st poly Si and leakage electric field E_1 on two measurement patterns.

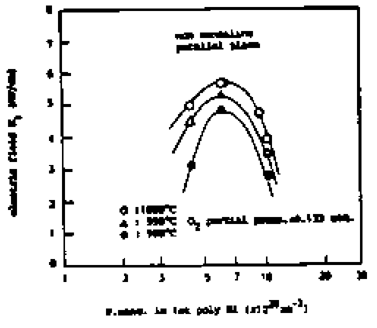


Fig.4 The relationship between the phosphorus concentration in 1st poly and leakage electric field E_1 at various oxidation temperature.

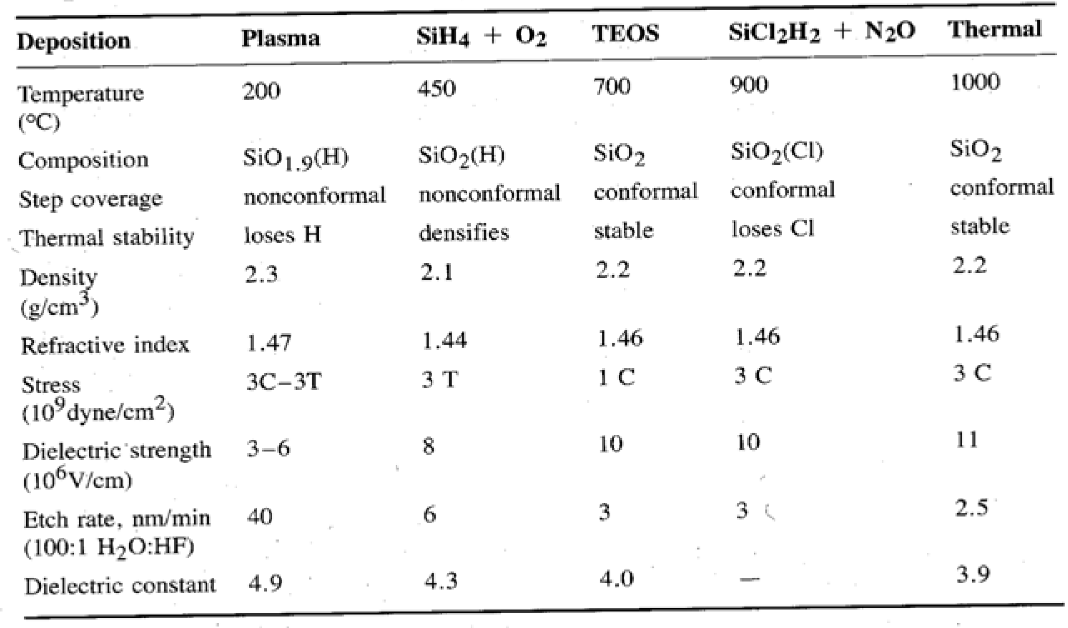
5. CVD SiO_2의 증착과 특성

(1) CVD Oxide 증착 (undoped)

장치	사용 개스	증착온도 (℃)	Step Coverage
APCVD	$SiH_4 + O_2$	400-450	poor
LPCVD	$SiH_4 + O_2$	400-450	good
	TEOS ($Si(OC_2H_5)_4$)	650-750	conformal
	$SiH_4 + 2N_2O$	750-850	conformal
	$SiCl_2H_2 + 2N_2O$	850-900	conformal
PECVD	$SiH_4 + O_2$	200-350	good
	$SiH_4 + N_2O$	200-350	good

(2) Typical CVD Oxide의 특성

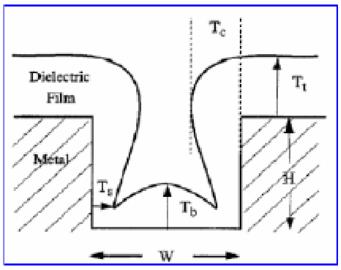
TABLE 3
Properties of silicon dioxide



Deposition	Plasma	$SiH_4 + O_2$	TEOS	$SiCl_2H_2 + N_2O$	Thermal
Temperature (°C)	200	450	700	900	1000
Composition	$SiO_{1.9}(H)$	$SiO_2(H)$	SiO_2	$SiO_2(Cl)$	SiO_2
Step coverage	nonconformal	nonconformal	conformal	conformal	conformal
Thermal stability	loses H	densifies	stable	loses Cl	stable
Density (g/cm^3)	2.3	2.1	2.2	2.2	2.2
Refractive index	1.47	1.44	1.46	1.46	1.46
Stress ($10^9 dyne/cm^2$)	3C-3T	3 T	1 C	3 C	3 C
Dielectric strength ($10^6 V/cm$)	3-6	8	10	10	11
Etch rate, nm/min (100:1 H_2O:HF)	40	6	3	3	2.5
Dielectric constant	4.9	4.3	4.0	—	3.9

* T: tensile, C: compressive

(3) Step Coverage of As-Deposited CVD Oxide Films


T_c
T_t
Dielectric Film
Metal
T_s
T_b
H
W

Aspect Ratio = H / W

Bottom step coverage = T_b / T_t

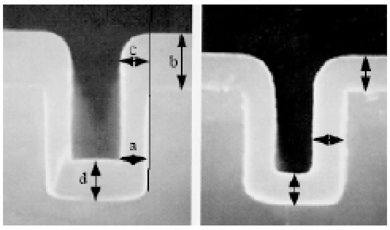
Side step coverage = T_s / T_t

Conformality = T_s / T_c

Step coverage definitions

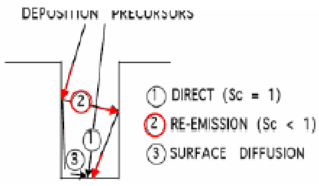
- Poor step coverage results from different deposition rates in parts of a microstructure.
- The profile of the thin film deposited by any of the CVD or PVD techniques depends upon :
  - Equipment configuration
  - Deposition method (SACVD, LPCVD, PECVD, PVD)
  - Reactant chemistry
  - Reactant transport mechanism

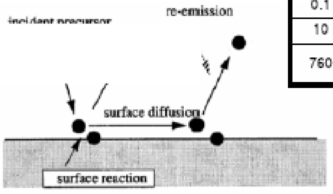
PETEOS vs O3 TEOS



Side step coverage	= a / b	= 50%	= 95%
Bottom step coverage	= d / b	= 65%	= 95%
Conformality	= a / c	= 85%	= 99%

▶ Sticking Coefficient


DEPOSITION PRECURSORS
②
①
③
① DIRECT (Sc = 1)
② RE-EMISSION (Sc < 1)
③ SURFACE DIFFUSION


incident precursor
re-emission
surface diffusion
surface reaction

$$S_c = \frac{\Gamma_{incident} - \Gamma_{re-emission}}{\Gamma_{incident}} = \frac{\Gamma_{reaction}}{\Gamma_{incident}}$$

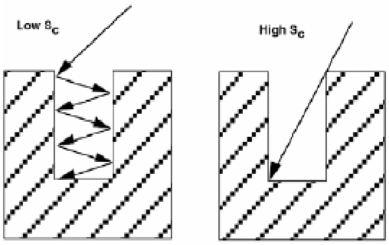
압력 (Torr)	밀도 (분자수/㎠)	Mean free path (㎛)	flux to surface (분자수/㎠sec.)
0.1	3.2E16	600	3.8E19
10	3.2E17	60	3.8E21
760	2.5E19	0.07	2.9E23

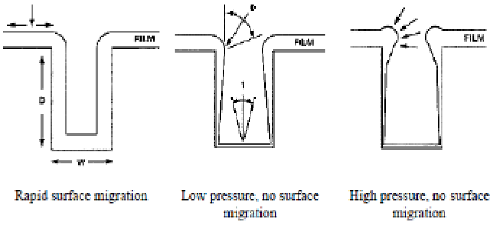
Transport of reactants to the surface at low pressure :

In most applications surface diffusion has been found to be negligible.

Sticking Coefficient : Sc

Reactive sticking coefficient is the probability of an incident deposition precursor…related to surface mobility.


Low S_c
High S_c


FILM
FILM
FILM
D
W

Rapid surface migration

Low pressure, no surface migration

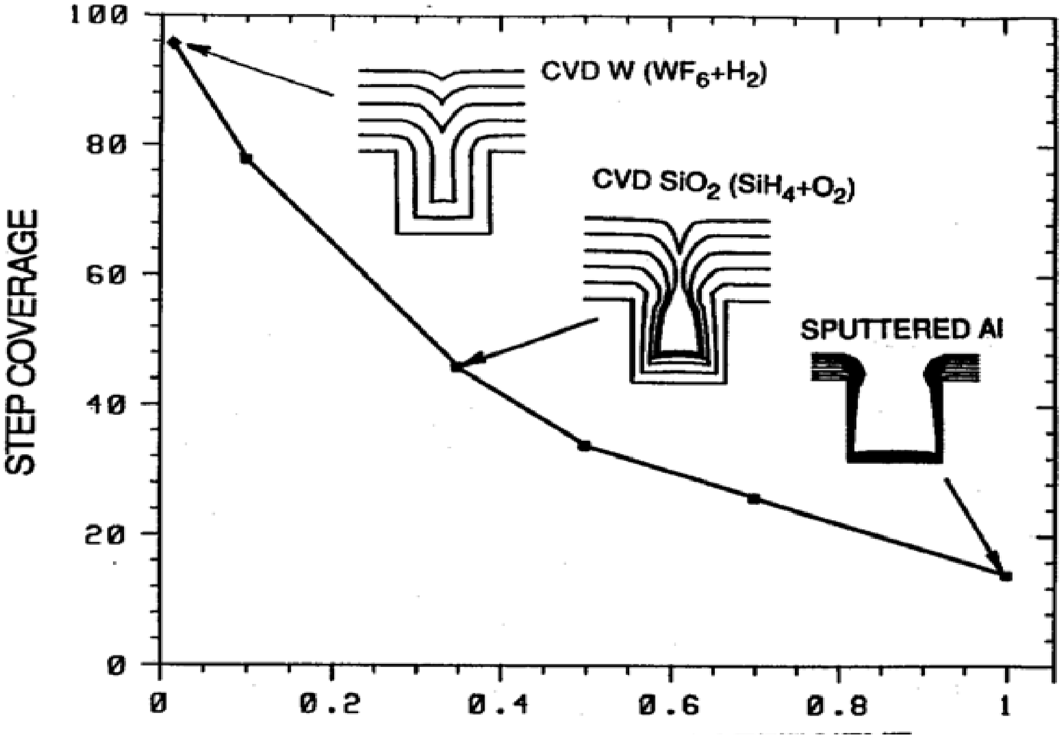
High pressure, no surface migration

☐ Sticking Coefficient

- **Step coverage can also be improved by changing** the slope of the walls.

- But this may result in an area penalty.

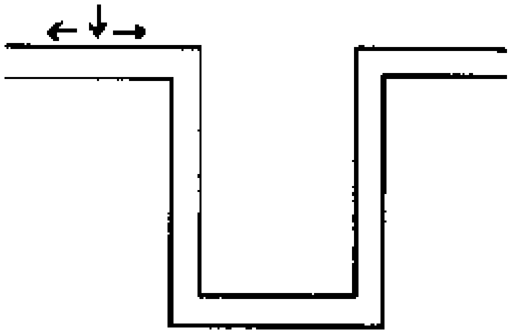
- Different lines show time evolution of the profile as simulated by the deposition and etch simulator SPEEDIE.



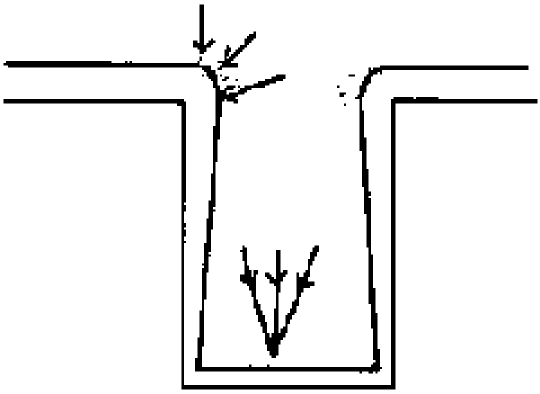
Sticking Coefficient

Material	Source	Temperature °C	Sc
PSG	SiH4 / O2 / PH3	400	0.35
SiO2	SiH4 / O2	400	0.26
SiO2	TEOS / O2	700	0.04
Poly-Si	SiH4	620 - 900	< 0.01
W	WF6 / H2	350 - 500	< 0.01

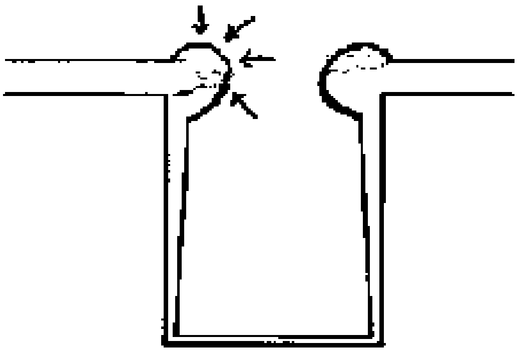
(i) TEOS Oxide, LPCVD, 650-850℃,
rapid surface migration



(ii) SiH_4 Oxide, PECVD, 350-400℃,
low pressure, no surface migration



(iii) SiH_4 Oxide, APCVD, 400-450℃
high pressure, no surface migration

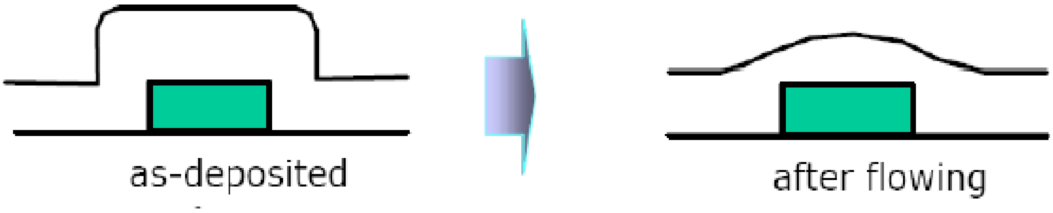


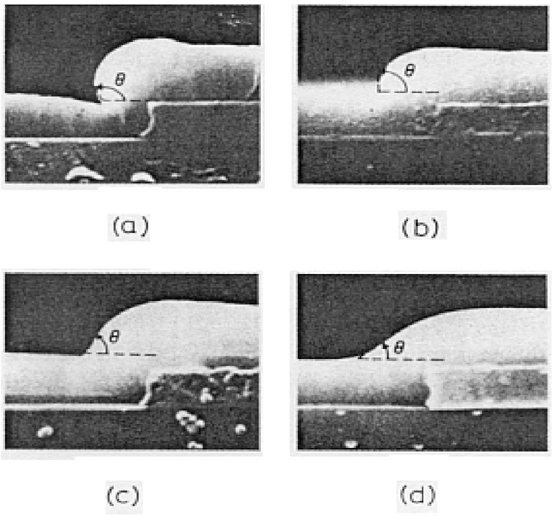
(4) Doped Oxide (Reflow glass)

□ **Reflow glass (PSG, BPSG)의 응용**

- Reflow glass가 사용되기 전에는 metal과 poly/diffusion의 isolation을 위하여 thermal oxide 또는 CVD oxide/nitride가 사용되었으나, sharp step과 re-entrant angle로 인하여 metal shorting 발생

- Reflow glass는 P, B등의 불순물이 도핑된 실리콘 산화막으로, 녹는 온도가 도핑이 안 된 순수한 실리콘 산화막의 녹는 온도 (1700℃)보다 월등히 낮아 (1000℃ 이하 가능), 증착한 후 reflow 시키면 smooth step을 얻을 수 있음





(a) (b)
(c) (d)

Fig. 19 SEM cross-sections (10,000X) of samples annealed in steam at 1100°C for 20 min for the following weight of phosphorus: (a) 0.0 wt.% P; (b) 2.2 wt.% P; (c) 4.6 wt.% P; 7.2 wt.% P.[33]

□ **Reflow glass의 장점**

– Smooth surface topology 형성

- Gettering and diffusion barrier to Na^+ ions, moisture
- Diffusion barrier to moisture

① PSG (PhosphoSilicate Glass)

□ 물질

- SiO_2와 P_2O_5 분자로 구성된 binary glass

□ 증착

장치	화학반응	온도(℃)
APCVD, PECVD	$SiH_4 + 6O_2 + 4PH_3$ -> $SiO_2 + 2P_2O_5 + 8H_2$	300-500

□ P 농도

- 6 ~ 8 wt% P
- 6 wt% 보다 낮을 때는 reflow가 잘 안됨
- 8 wt% 보다 높을 때는 PSG의 습윤성이 증가 => 습기를 흡수하여 H_2PO_4(인산)을 형성 => metal 부식이 발생

□ reflow 조건

- 1000 ~ 1100 ℃, 10 ~ 30 분, H_2O, N_2, O_2 분위기
- Step angle: 25 - 55 °

② BPSG (BoroPhosphoSilicate Glass)

□ 물질: SiO_2, P_2O_5, B_2O_3 분자들로 구성된 ternary glass

□ 특성

- Chemistry : $Si(OC_2H_5)_4 + O_3/O_2 + B(OC_2H_5)_3 + PO(OC_2H_5)_3) \rightarrow SiO_2\ (B,P) + H_2O\uparrow + CO_2\uparrow$
- Void-free gap filling with 고온 reflow (>800 ℃)

- 단점

- High Wet Etch Rate (100:1 HF : 200 Å/min)
- Liner SiN consume
- Low Temp.(<800 ℃) anneal 시 void 발생

- Applications

- ILD, mold oxide

□ 증착

장치	화학반응	온도(℃)
APCVD PECVD	$SiH_4 + 9O_2 + 4PH_3 + 2B_2H_6 \rightarrow SiO_2 + 2P_2O_5 + 2B_2O_3 + 14H_2$	300-500

□ B, P 농도

- B: 5 wt%, P: 5wt%
- 농도가 지나치게 높으면 습윤성이 높아 H_2PO_4(인산) 및 BPSG crystal 형성 가능

□ reflow 조건

- 800 - 900 ℃, 30 - 60 min., H_2O, N_2 분위기

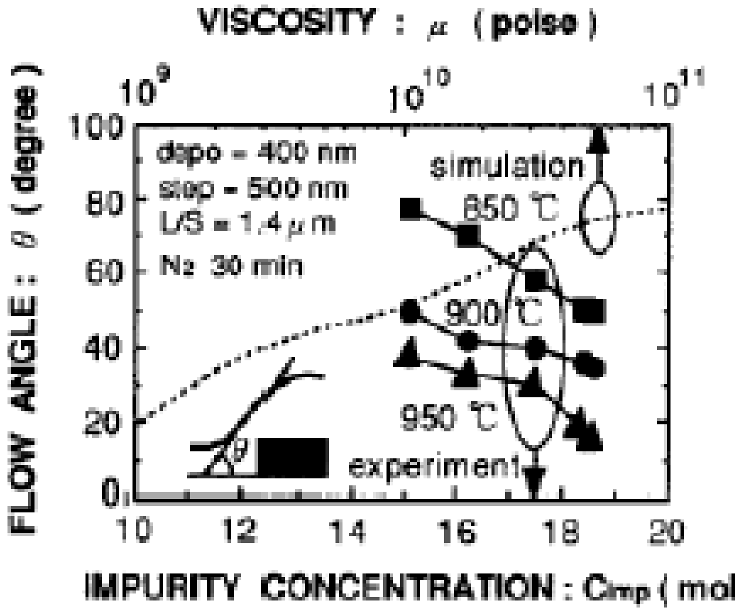


Fig. 1 The measured flow angle versus impurity concentration in the line structure. The simulated flow angle is a function of the viscosity of BPSG.

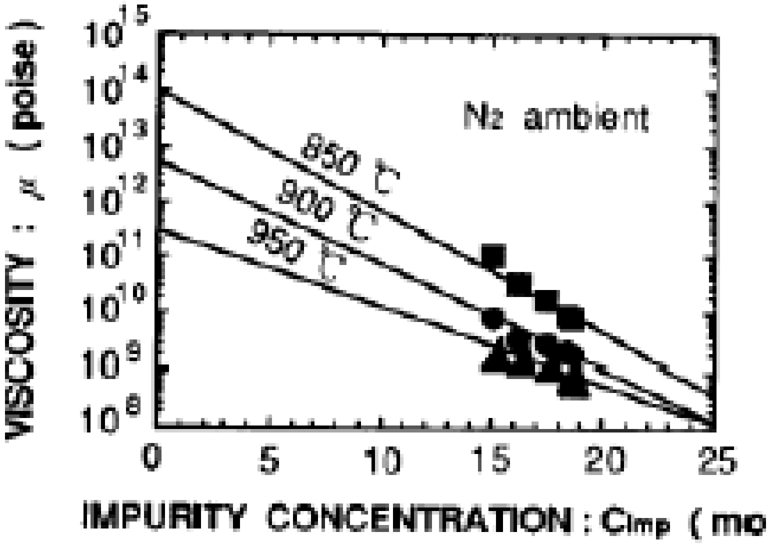


Fig. 2 Viscosity of BPSG versus impurity concentration. Viscosity is a function of the temperature and impurity concentration.

6. CVD Si_3N_4의 증착과 특성

(1) CVD Nitride 박막의 증착

장치	화학반응	증착온도(℃)	응용
LPCVD	$SiCl_2H_2$ + NH_3	650-750	LOCOS, MNOS
	SiH_4 + NH_3	700-900	
PECVD	SiH_4 + NH_3	200-350	Passivation
	SiH_4 + N_2	200-350	

(2) CVD Nitride 박막의 특성

- 내산화성이 강함
- Good barrier to diffusion of Na, H_2O
- 경도가 높다: scratch 방지
- 높은 유전율 (ε_r = 6 - 9, 반면에 4.2 for CVD Oxide). 그러므로, ILD로 사용은 부적당

- high stress of film: 2000Å 이상이면 crack 가능
  LPCVD nitride: 1.2 - 1.8 x10^{10} dyne/cm^2 (tensile)
  PECVD nitride: 1- 8 x10^9 dyne/cm^2 (compressive)

- 수소 함유량이 높다
  LPCVD nitride: 8 wt%
  PECVD nitride: 18 - 22 wt% with use of NH_3
  * 고농도의 수소 함유는 MOS의 문턱 전압의 변동, nitride 막의 에칭 특성의 변화를 가져오며, 또한 nitride 막을 사용한 H_2 passivation 가능

- LPCVD nitride is stoichiometric and a good barrier against oxidation and sodium diffusion.
- PECVD nitride contains a large amount of hydrogen and can be etched with HF.

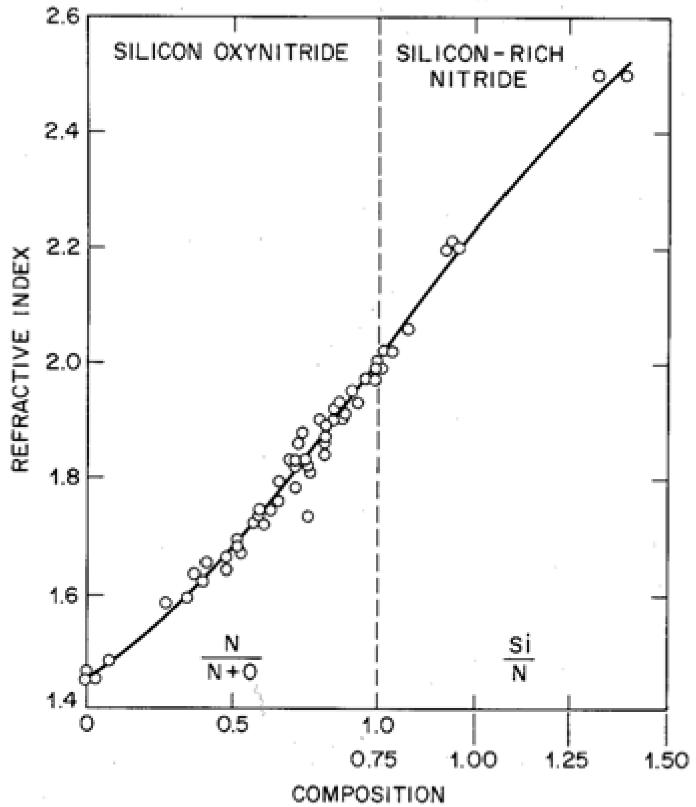
7. CVD Oxynitride and SIPOS

(1) Oxynitride

- Source gas: $SiH_4 + N_2O + NH_3$
- Good barrier to moisture and Na
- Good for Passivation

(2) SIPOS (Semi-insulating polycrystalline silicon)

- silicon-rich oxide film (SiO_x: $0.48 < x < 2$)
- good passivation layer for high field transistor



8. HDP CVD (High Density Plasma CVD)

- PE-CVD 보다 저압에서 ICP type high density plasma source 사용

- Plasma density 증가 ➔ Ion density 증가 > 1% (std PE-CVD < 0.01%)

- Mean free path 증가

- Back bias 에 따른 depo & sputtering ratio 변경가능

- 장점

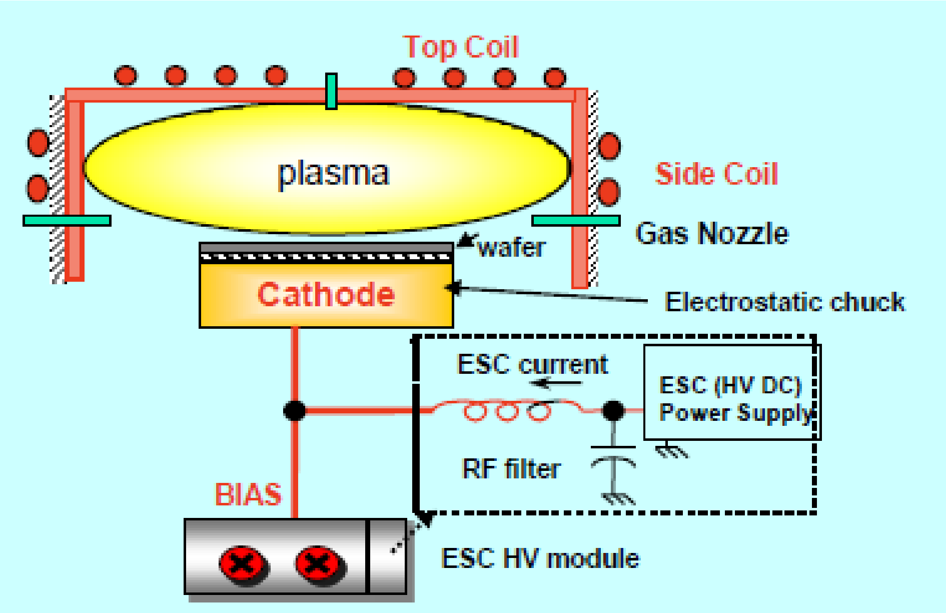
- Better Mechanical strength than PE-CVD
- High Quality SiO_2
- Dopant control 용이 (ex. PSG, FSG)

- 단점

- Plasma damage

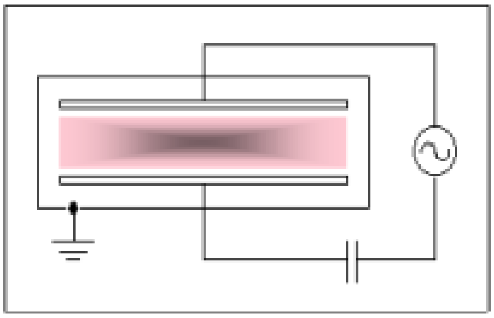
- 용도

- STI, ILD, IMD filling


Top Coil
plasma
Side Coil
Gas Nozzle
wafer
Cathode
Electrostatic chuck
ESC current
ESC (HV DC) Power Supply
RF filter
BIAS
ESC HV module

Inductive Coupled Plasma

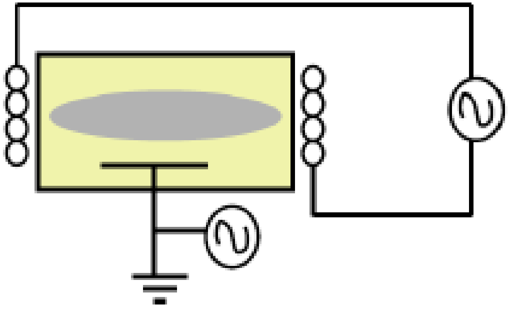
Capacitively Coupled Plasma



Plasma Enhanced CVD

- P<10Torr
- Ion density <0.01%
- Low cost

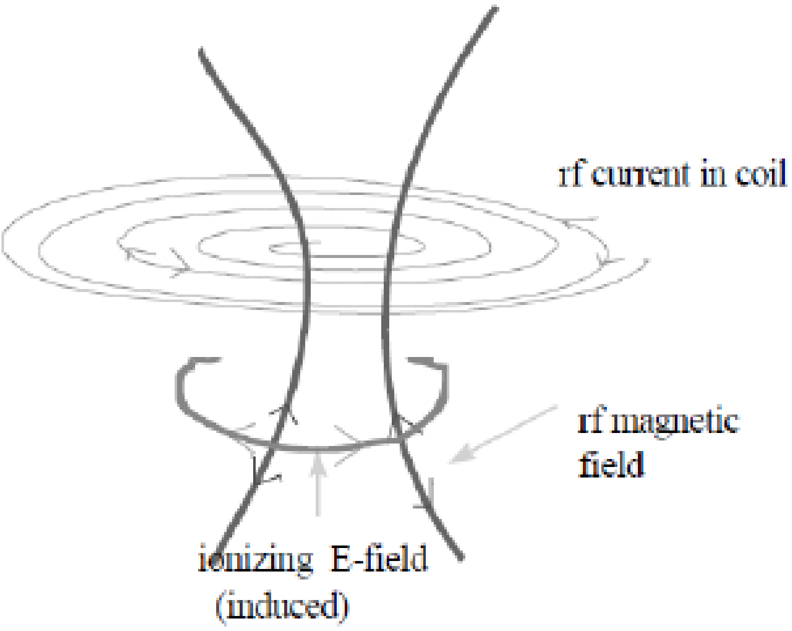
Inductively Coupled Plasma



High Density Plasma CVD

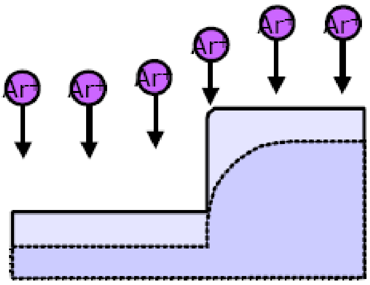
- P~ mTorr (turbo pump)
- Ion density >1%

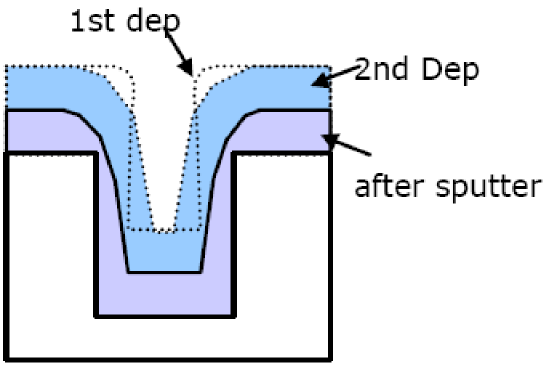
Inductive Coupling:


rf current in coil
rf magnetic field
ionizing E-field (induced)

□ HDP CVD – continued

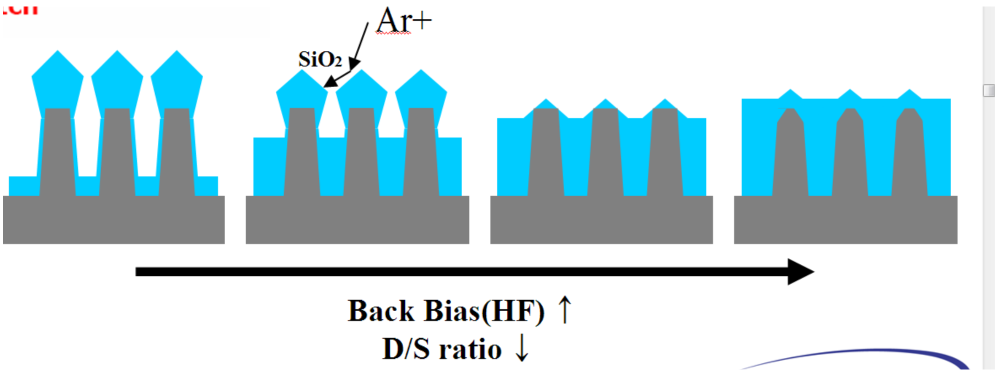
- **Chemistry :**
  $SiH_4 + 2O_2 + Ar(\text{or He}) \rightarrow SiO_2 + 2H_2O\uparrow + Ar(\text{or He})\uparrow$
- **Stress: –1.5E9 dyne/cm^2(STI, ILD), –1.0E9 dyne/cm^2 (IMD)**
- **Wet Etch Rate : 50 Å/min @ 100:1 HF**
- **Bias Power 증가 시 : Sputter rate ↑,**
  wafer temp ↑, Plasma damage ↑
- **공정 관리 point ; DS ratio (D/R, Sputter rate)**


Ar
Ar
Ar
Ar
Ar
Ar


1st dep
2nd Dep
after sputter

Dep & Etch

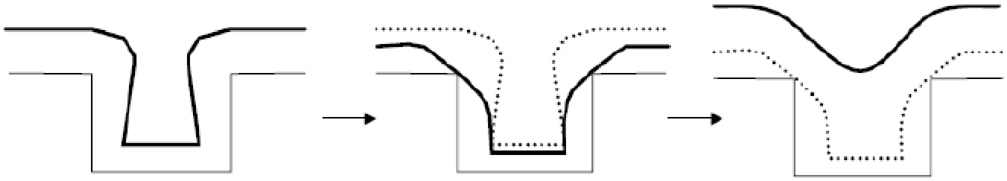
▶ D/S ratio에 따른 **profile** 변화


Ar+
SiO2
Back Bias(HF) ↑
D/S ratio ↓

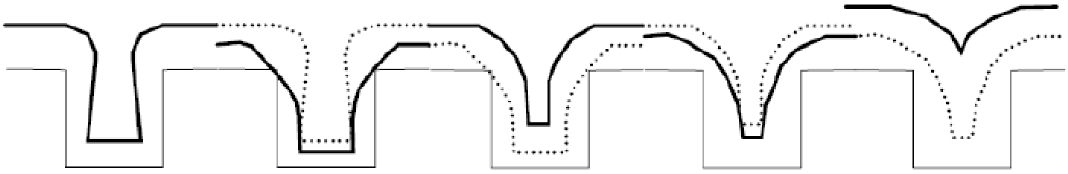
* $$D/S\,ratio = \frac{\text{증착속도} + \text{에칭속도}}{\text{에칭속도}}$$

- **Depo/etch/depo gap-fill 특성**

depo → etch → depo



depo → etch → depo → etch → depo → · · ·



9. 도포법에 의한 절연막 증착

• 회전 도포와 bake process를 통하여 절연막을 형성하는 기술로서 평탄화 능력이 아주 우수. 대표적인 재료로는 SOG와 polymide 수지막이 있다.

(1) SOG (Spin-On-Glass)

(a) SOG 수용액
- Siloxane or Silicate
- Alcohol-based solvent (에스테르, 케톤 등)
- 유기 binder {methyl(CH_3) or phenyl(C_6H_5)}: crack 방지
- 인화합물 (P_2O_5): gettering, crack 방지

(b) 장점

- ILD without no void	- 공정이 단순
- 결함 밀도가 낮다	- 생산성이 높다
- 공정 비용이 낮다	- no 유독성 가스

(c) 단점
- Out-gassing 문제 발생 가능: VIA의 contact 저항 증가 (SOG 내에 잔존하고 있는 수분에 의해 발생)
- high tensile stress: crack 가능
- metal, resist layer와의 접착력이 나쁨

(d) SOG 증착 공정

① Dispense & Spin

- 수용액의 점도, 회전수에 의해 박막두께/두께 균일도가 결정됨

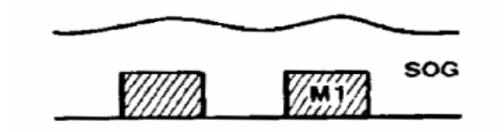
② Cure

- 저온 bake (150-250℃, 1-15 min) + 고온 bake (400-425℃, 30-60 min)

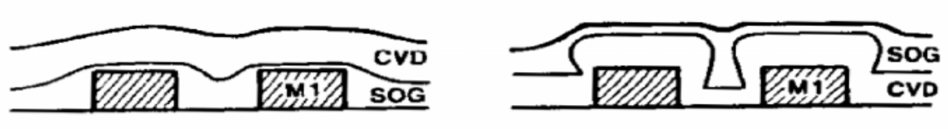
- Solvent, moisture가 증발하면서 silanol (SiOH) group이 polymerization되면서 SiO_2 막을 형성 => 심각한 mass loss로 인해 막이 shrink => 높은 tensile stress 발생

(e) SOG Process Integration

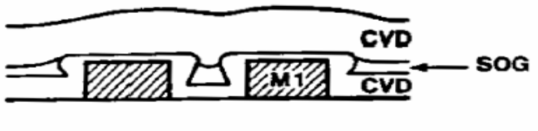
- 일반적으로 SOG는 sandwich-type: ILD_1/SOG/ILD_2
- SOG 만을 사용하는 경우 지나치게 두꺼워 crack이 발생 가능
- SOG 위에 ILD_2가 없는 경우 metal/resist 사이 접착력 문제 발생



A: SOG STANDALONE



B: CVD/SOG COMPOSITE



C: CVD/SOG/CVD COMPOSITE
WITH PARTIAL SOG ETCH-BACK

(i) SOG Etchback 공정

장점: no poisoned VIA

단점: complex process, thick ILD_1 film

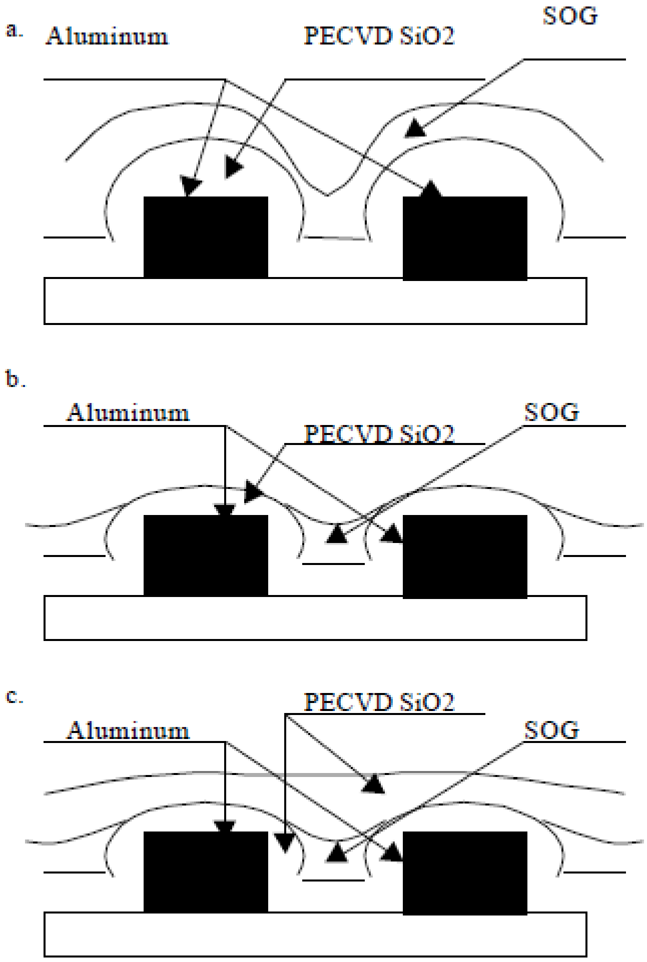

a.
Aluminum
PECVD SiO2
SOG
b.
Aluminum
PECVD SiO2
SOG
c.
PECVD SiO2
Aluminum
SOG

Figure 1. Three steps in SOG processing: a) SOG spin-on, b) etchback step, c) top layer of PECVD SiO2.

(ii) SOG Non-etchback process

- Process flow
  - ① Metal 1 deposition/ pattern/ etching/ PR strip
  - ② ILD$_1$ deposition: 2000Å oxynitride
  - ③ Spin 1: 2200Å SOG
  - ④ Spin 2: 2200Å SOG
  - ⑤ SOG Cure 1: 425℃, 60 min
  - ⑥ ILD$_2$ deposition: 4000Å LTO, 425℃
  - ⑦ VIA pattern/ etching/ PR strip
  - ⑧ SOG Cure 2: 425℃, 60 min, O$_2$
  - ⑨ Metal 2 deposition/ pattern/ etching/ PR strip

- 장점: 공정 단순
  단점: poisoned VIA 발생 가능

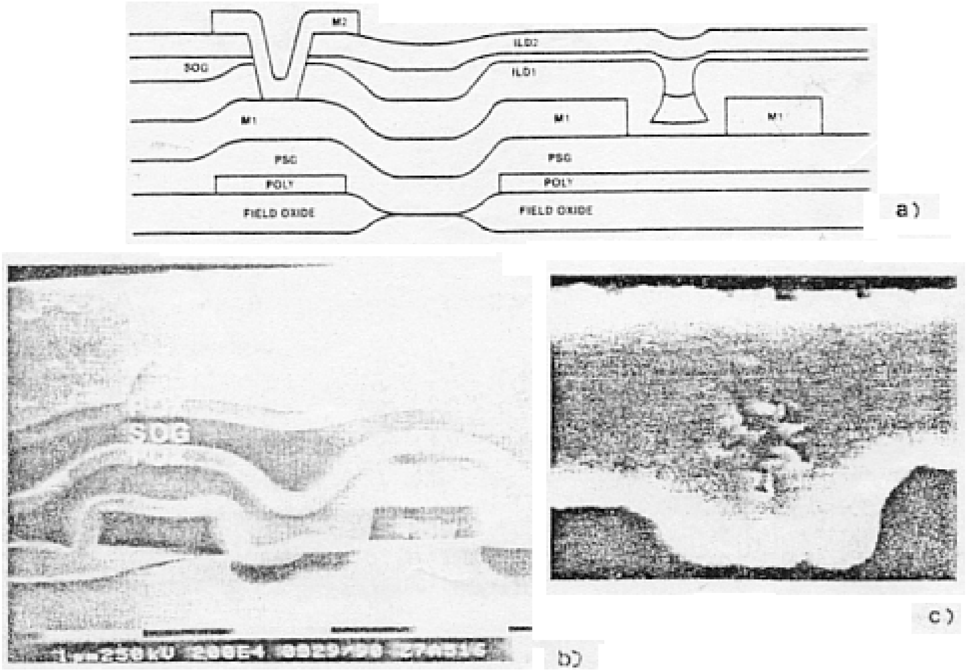

M2
ILD2
SOG
ILD1
M1
M1
M1
PSG
PSG
POLY
POLY
FIELD OXIDE
FIELD OXIDE
a)
SOG
b)
c)

Fig. 4-33 (a) Drawing of a cross-section of structure formed using the non-etchback SOG process. (b) SEM micrograph of a structure formed with the non-etchback SOG process. Courtesy of Allied-Signal, Inc. (c) SEM micrograph of a cross section of a "poisoned via."[92] (© 1987 IEEE).

10. Atomic Layer Deposition (ALD)

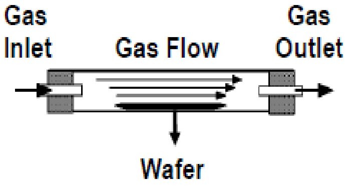
- CVD 대비 Step Coverage 및 두께 조절 능력 우수 (특히 수 Å 단위의 Thin Layer)

- CVD 대비 Chamber Volume이 작음

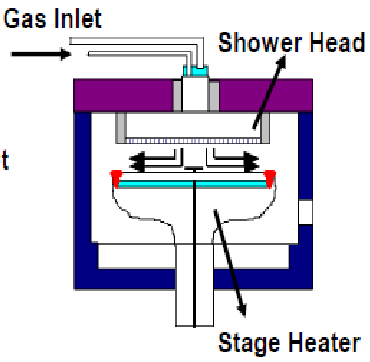
- ALD는 Hardware 구성 방법에 따라, Traveling Wave 및 Shower Head Type으로 구분함

- ALD는 사용하는 Source 분해 원에 따라 Thermal ALD 및 PE ALD (Plasma Enhanced ALD)으로 구분함

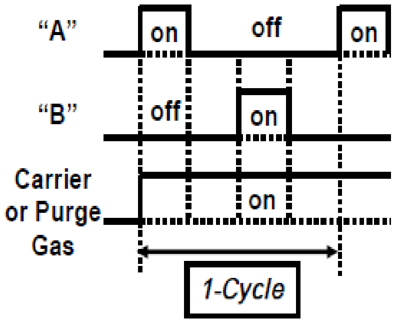
- Throughput 개선을 위하여, Pseudo-ALD 공정이 나옴


Gas
Inlet
Gas Flow
Gas
Outlet
Wafer

Traveling Wave


Gas Inlet
Shower Head
Stage Heater

Shower Head


"A"
on
off
on
"B"
off
on
Carrier
or Purge
Gas
on
1-Cycle

❑ ALD 공정이 가능한 물질

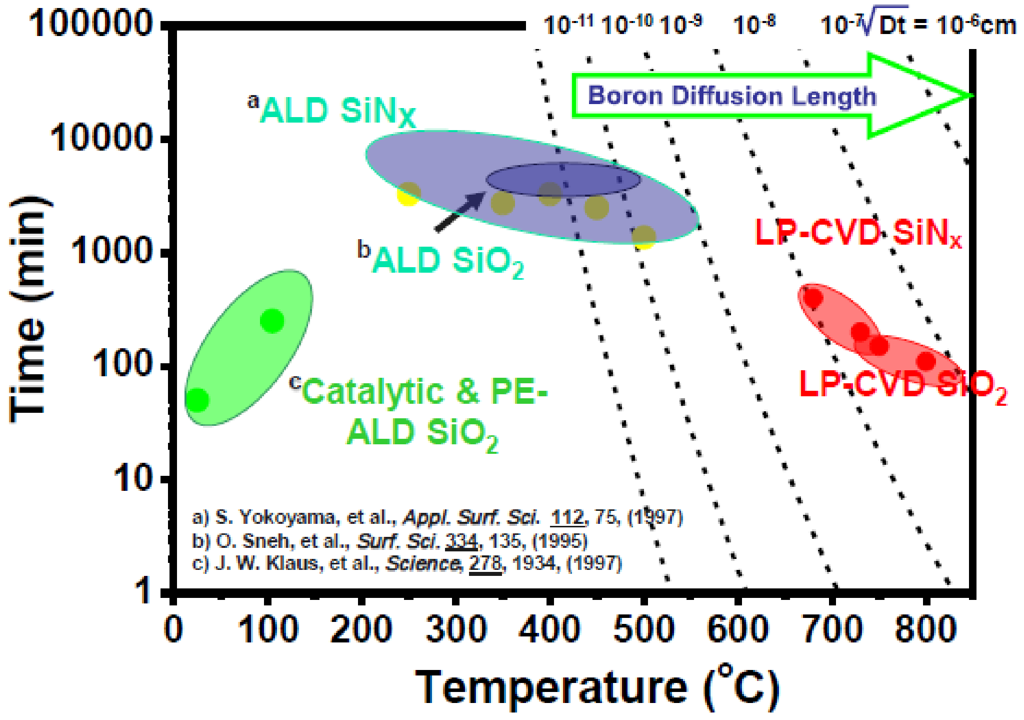
Dielectrics	SiO_2, Al_2O_3, TiO_2, ZrO_2, HfOx, Ta_2O_5, MgO, CeO_2
Transparent Conductors	In_2O_3, In_2O_3:Sn, In_2O_3:F, In_2O_3:Zr, SnO_2, SnO_2:Sb, ZnO, ZnO:Al
II-VI Compounds	ZnS, ZnSe, ZnTe, ZnSSe, CaS, SrS, BaS, CdS, CdTe, HgTe, HgCdTe
Nitrides	SiN, AlN, GaN, InN, TiN, TaN, TiAlN, TiSiN, WN, WCN
Fluorides	CaF_2, SrF_2, ZnF_2
Pure Metal	Cu, Al, Mo, Ti, W, Co, Ni

[Film Properties of Various Deposition Method]

	PVD	CVD	PECVD	ALD
Atomically Fine Thickness Control	Difficult	Difficult	Difficult	Easy
Method of Thickness Control	Time	Time	Time	Cycle
Large Area Growth	Moderate	Moderate	Difficult	Easy
Growth Temperature	Low	High	Moderate	Moderate
Step Coverage	Bad	Good	Moderate	Excellent
Throughput	High	Moderate	Moderate	Low

• Why ALD Needed?

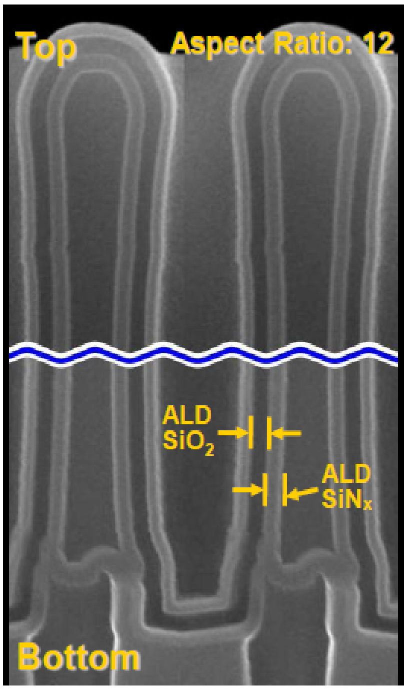
Thermal Budget and Boron Diffusion Length



- ALD process suppresses dopant diffusion.

- **Why ALD Needed?**

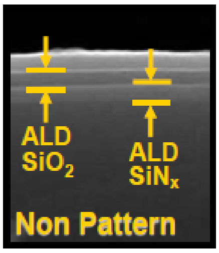
Step Coverage & Pattern Loading


Top
Aspect Ratio: 12
ALD SiO_2
ALD SiN_x
Bottom

ALD SiN_x : 595°C
ALD SiO_2 : 105°C

- Step Coverage : > 98%

- Pattern Loading : > 98%


ALD SiO_2
ALD SiN_x
Non Pattern

□ **ALD SiO_2**

- “Si” 과 “O” source 교차 주입에 의한 film 형성
- 장점: 저온 공정, step coverage 우수, 두께 조절 용이
- 단점: High wet etch rate, low dep. Rate
- 용도: Oxide spacer, sacrificial oxide

Properties	ALD SiO2	O3-TEOS USG
Chemistry	Chloro-silane Amino-silane	TEOS, O3/O2
Temp. (℃)	RT ~ 600C	550
Pressure (Torr)	0.5 ~1.5	600
Step coverage	>95%	95%