Schematic cross section of n-MOSFET
Wafer Cleaning

1 Organics
H₂SO₄ +
H₂O₂
H₂O Rinse

2 Oxides
HF +
H₂O
H₂O Rinse

3 Particles
NH₄OH +
H₂O₂ + H₂O
H₂O Rinse

4 Metals
HCl +
H₂O₂ + H₂O
H₂O Rinse

5 Dry
H₂O or IPA +
N₂

Wet station
Spin dryer
Thermal Oxidation
A process to form a thermal SiO$_2$ thin film

Dry oxidation: slow but dense film

\[
\text{Si (s) } + \text{O}_2 (g) \rightarrow \text{SiO}_2 (s)
\]

900 ~ 1200 °C, 1 atm

Wet oxidation: fast but less dense film

\[
\text{Si (s) } + 2\text{H}_2\text{O}(g) \rightarrow \text{SiO}_2 (s) + 2\text{H}_2(g)
\]

900 ~ 1200 °C, 1 atm
Chemical Vapor Deposition
Vacuum deposition of thin film (SiO$_2$, Si$_3$N$_4$, poly-Si, etc)

SiO$_2$ film: $\text{SiH}_4 (g) + \text{O}_2(g) \rightarrow \text{SiO}_2 (s) + 2\text{H}_2(g)$  

Si$_3$N$_4$ film: $3\text{SiCl}_2\text{H}_2 (g) + 4\text{NH}_3(g) \rightarrow \text{Si}_3\text{N}_4 (s) + 6\text{HCl} (g) + 6\text{H}_2(g)$  

Poly-Si film: $\text{SiH}_4 \rightarrow \text{Si}(s) + 2\text{H}_2(g)$
Physical Vapor Deposition
Metallization for interconnection (Aluminum)

Thermal evaporation

E-beam evaporation

Sputtering
Chemical-Mechanical Polishing (CMP)
A process for planarization due to the multilevel interconnection
Photolithography

A process to make a pattern of a film

- Critical dimension (CD):
  \[ CD \approx \sqrt{\lambda g} \]
  \( \lambda \): wavelength
  \( g \): gap
<table>
<thead>
<tr>
<th>Step</th>
<th>Operation</th>
<th>Process</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PR coating</td>
<td>Apply PR on a substrate by spin coating</td>
</tr>
<tr>
<td>2</td>
<td>Soft baking</td>
<td>Low temperature cure to dry resist</td>
</tr>
<tr>
<td>3</td>
<td>Exposure</td>
<td>Align and expose to selectively polymerize the PR</td>
</tr>
<tr>
<td>4</td>
<td>Development</td>
<td>Dissolve the un-polymerized PR</td>
</tr>
<tr>
<td>5</td>
<td>Inspection</td>
<td>Verify accurate image transfer to PR</td>
</tr>
<tr>
<td>6</td>
<td>Post-exposure</td>
<td>Higher temperature cure to completely dry and polymerize the PR. (also</td>
</tr>
<tr>
<td></td>
<td>baking</td>
<td>called “hard baking”)</td>
</tr>
<tr>
<td>7</td>
<td>Etching</td>
<td>Form a patterned film</td>
</tr>
<tr>
<td>8</td>
<td>PR strip</td>
<td>Remove the PR pattern</td>
</tr>
<tr>
<td>9</td>
<td>Inspection</td>
<td>Verify accurate image transfer to the film</td>
</tr>
</tbody>
</table>
**Positive PR**

- Positive resists **decomposes** by being exposed by UV light.
- Exposure to the UV light changes the chemical structure of the resist so that it becomes *more soluble* in the developer.
- The unexposed region will be polymerized by soft and hard baking.

**Negative PR**

- Exposure to the UV light causes the negative resist to become **polymerized**, and more difficult to dissolve.
- Therefore, the negative resist remains on the surface wherever it is exposed, and the developer solution removes only the unexposed portions.
- Masks used for negative photoresists, therefore, contain the inverse (or photographic "negative") *of the pattern to be transferred.*
Etching

- Etching is the process where unwanted areas of films are removed by either dissolving them in a wet chemical solution (Wet Etching) or by reacting them with gases in a plasma to form volatile products (Dry Etching).

- **Isotropic etch**
  - a process that etches at the same rate in all directions.

- **Anisotropic etch**
  - a process that etches only in one direction.
Wet Etching

- For SiO$_2$ etching
  - HF + NH$_4$F+H$_2$O (buffered oxide etch or BOE)
- For Si$_3$N$_4$
  - Hot phosphoric acid: H$_3$PO$_4$ at 180 °C
  - need to use oxide hard mask
- Silicon
  - Nitric, HF, acetic acids
  - HNO$_3$ + HF + CH$_3$COOH + H$_2$O
- Aluminum
  - Acetic, nitric, phosphoric acids at 35-45 °C
  - CH$_3$COOH+HNO$_3$+H$_3$PO$_4$
Dry Etching

- \( \text{SiO}_2 \): \( \text{CF}_4/\text{CHF}_3/\text{Ar} \)
- \( \text{Si}_3\text{N}_4 \): \( \text{CHF}_3/\text{O}_2 \)
- \( \text{Silicon} \): \( \text{HBr}/\text{NF}_3/\text{O}_2/\text{SF}_6 \)
- \( \text{Aluminum} \): \( \text{BCl}_3/\text{Cl}_2 \)
Impurity Doping

A process to introduce a controlled amount of impurity atoms to Si

**Diffusion**

- Gas of dopant atoms
- Mask
- \( \ln C \) vs. \( x \)
- \( \text{N}_2 + \text{O}_2 \) to \( \text{POCl}_3 \)

**Implantation**

- High-velocity dopant ions
- Mask
- \( \ln C \) vs. \( x \)

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Prof. Yo-Sep Min

Electronic Materials: Semiconductor Physics & Devices

Chapt. 4 - Lec 23-14
Individual integrated circuits are tested to distinguish good die from bad ones.
Good chips are attached to a lead frame package.
Die Attach and Wire Bonding

- lead frame
- gold wire
- bonding pad
- connecting pin
Final Test

Chips are electrically tested under varying environmental conditions.
Moore’s Law

- **Moore's law** is the observation that the number of transistors on IC doubles approximately every two years.
- The law is named after Intel co-founder Gordon E. Moore, who described the trend in his 1965 paper.
Announcements

• Homework problem set (due to Dec. 15):
  18. 2; 18.6; 18.15

• Final EXAM: Dec. 15, 13:00 ~ 15:00, 별 232
  Everything studied after the Mid-Term EXM