CHAPTER 8

Combinational Circuit design and Simulation Using Gate

This chapter in the book includes:

Objectives

Topics introduced in this chapter:

- Draw a timing diagram for a combinational circuit with gate delays.
- Define static 0-and 1-hazards and dynamic hazard. Given a combinational circuit, find all of the static 0-and 1-hazards. For each hazard, specify the order in which the gate outputs must switch in order for the hazard to actually produce a false output.
- Given switching function, realize it using a two-level circuit which is free of static and dynamic hazards (for single input variable changes).
- Design a multiple-output NAND or NOR circuit using gates with limited fan-in.
- Explain the operation of a logic simulator that uses four-valued logic.
- Test and debug a logic circuit design using a simulator.

8.2 Design of Circuits with Limited Gate Fan-in

Example: Realize $f(a,b,c,d) = \sum m(0,3,4,5,8,9,10,14,15)$ using 3-input NOR gate

map of f:

cd \ ab	00	01	11	10
00	1	1	0	1
01	0	1	0	1
11	1	0	1	0
10	0	0	1	1

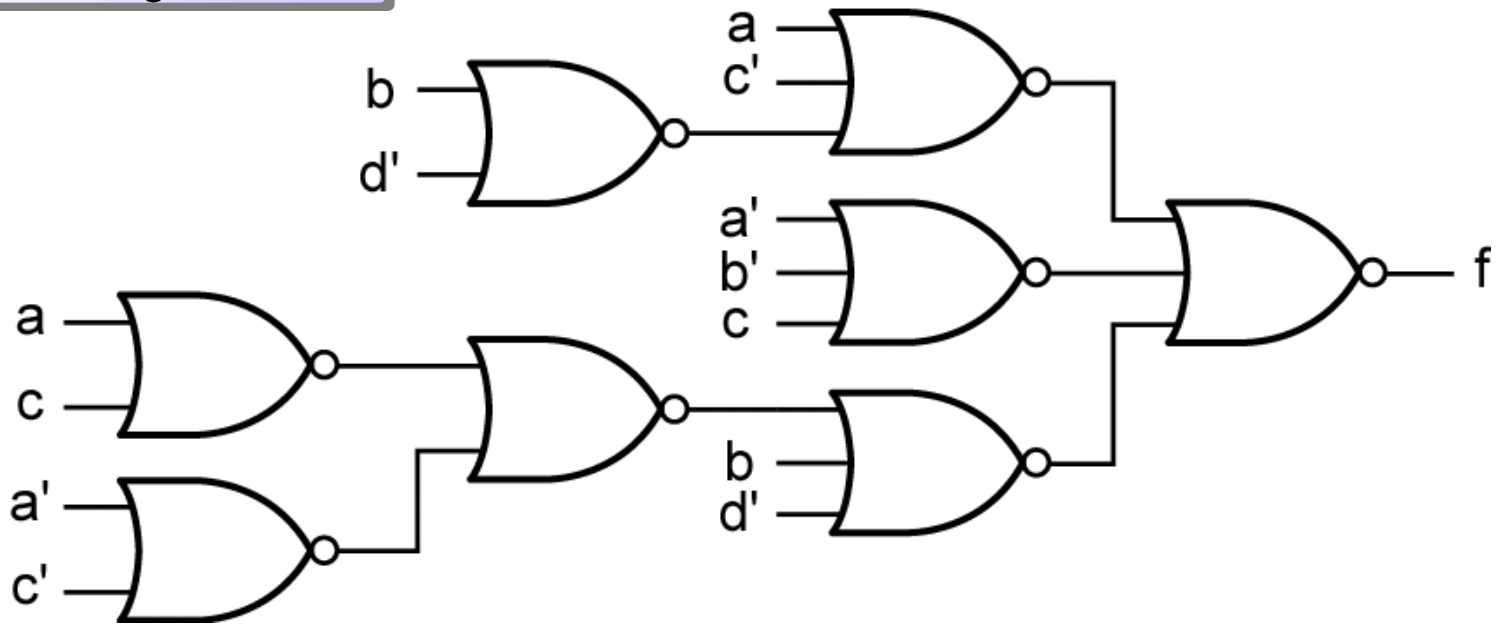
$$f' = a'b'c'd + ab'cd + abc' + a'bc + a'cd'$$

8.2 Design of Circuits with Limited Gate Fan-in

$$f' = b'd(a'c'+ac) + a'c(b+d') + abc'$$

$$f = [b+d'+(a+c)(a'+c')][a+c'+b'd][a'+b'+c]$$

Resulting NOR-gate of ***f***



8.2 Design of Circuits with Limited Gate Fan-in

Example: Realize the functions given in Figure 8-2,

using only 2-input NAND gates and inverters.

If we minimize each function separately, the result is

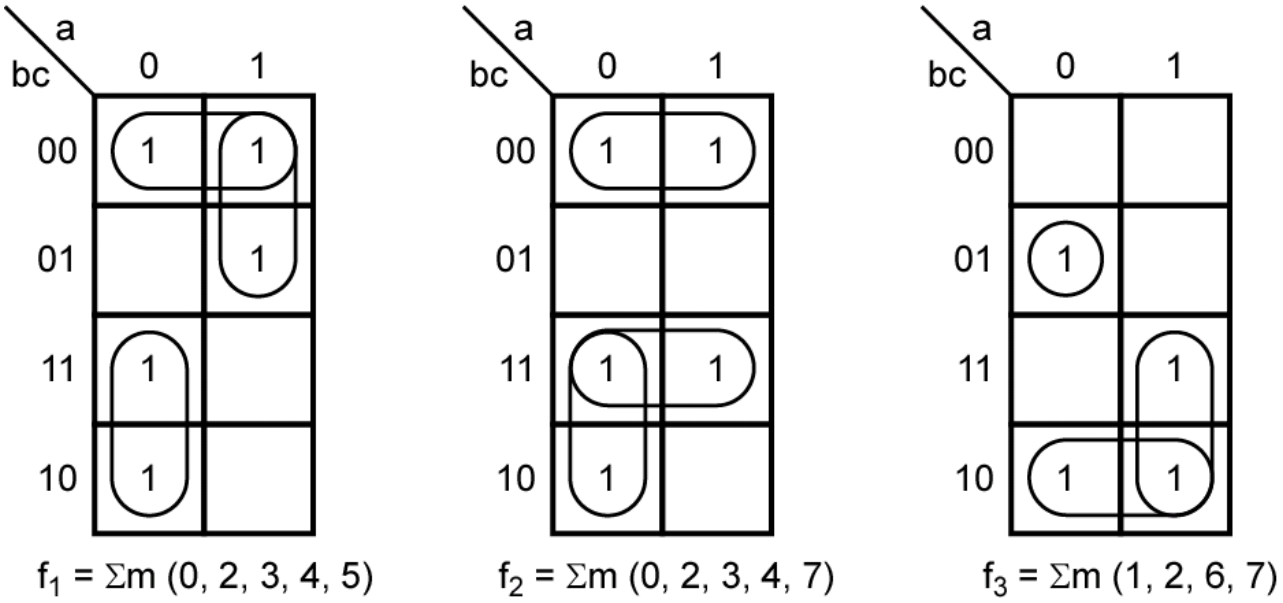


Figure 8–2

Result

$$f_1 = b'c' + ab' + a'b$$

$$f_2 = b'c' + bc + a'b$$

$$f_3 = a'b'c + ab + bc'$$

8.2 Design of Circuits with Limited Gate Fan-in

$$f_1 = b'(\underline{a+c'}) + \underline{a'b}$$

$$f_2 = (b'+c)(b+c') + \underline{a'b} \quad (or \quad f_2 = b(a'+c) + \underline{b'c'})$$

$$f_3 = a'b'c + b(\underline{a+c'})$$

eliminate the remaining 3-input gate by Eq. $a'b'c = a'(b'c) = a'(b+c')'$

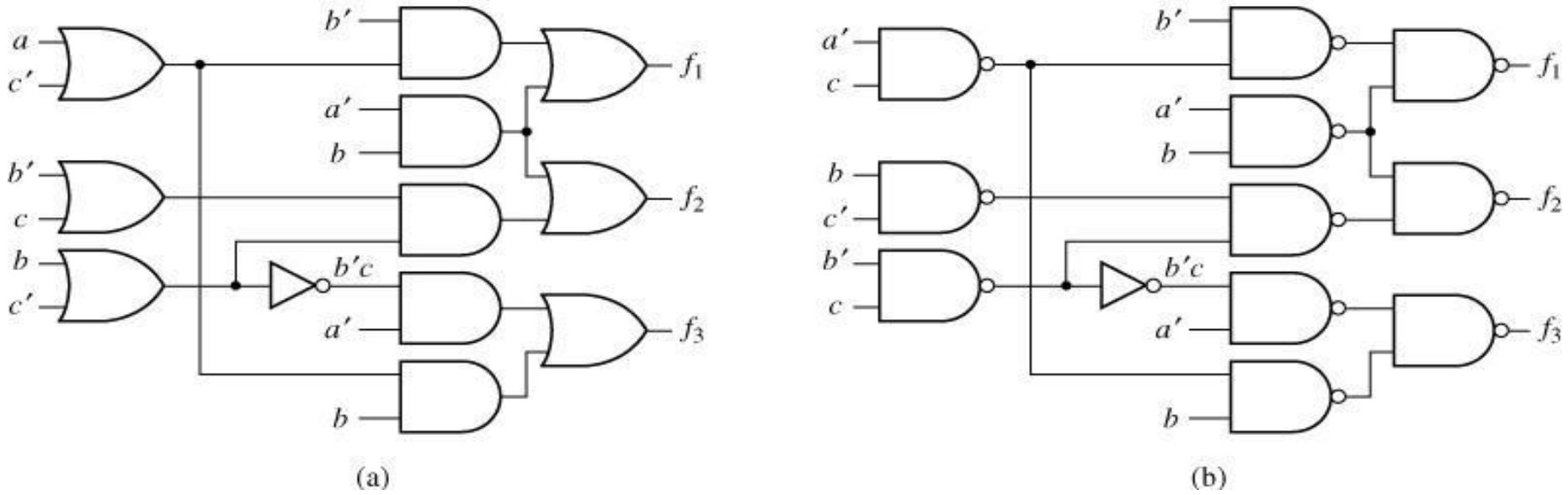
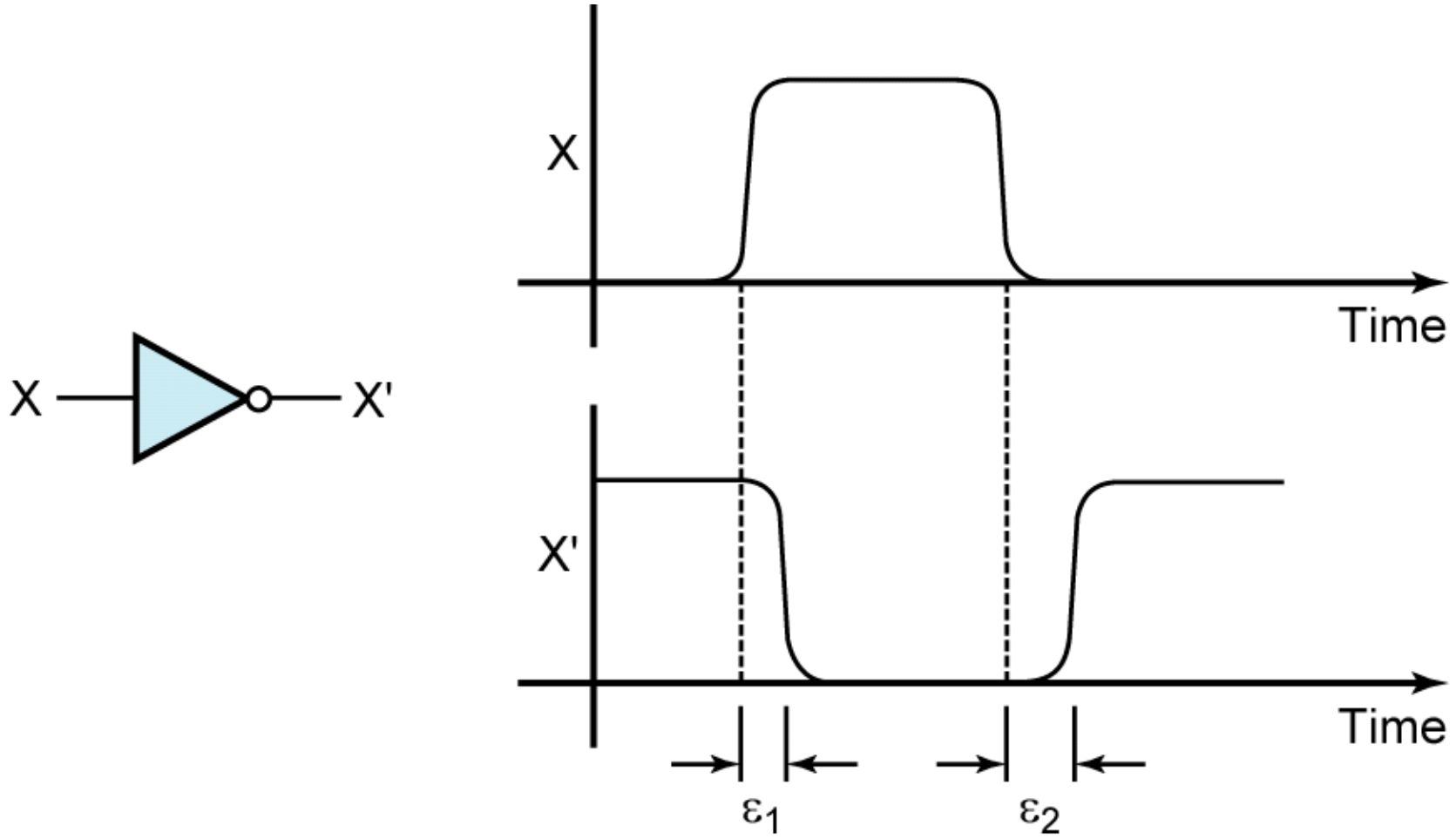


Figure 8-3: Realization of Figure 8-2

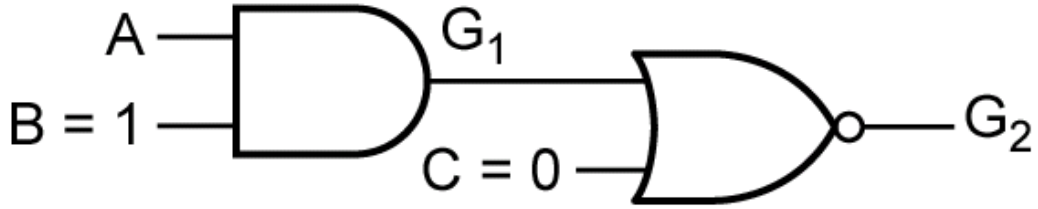
8.3 Gate Delays and Timing Diagrams

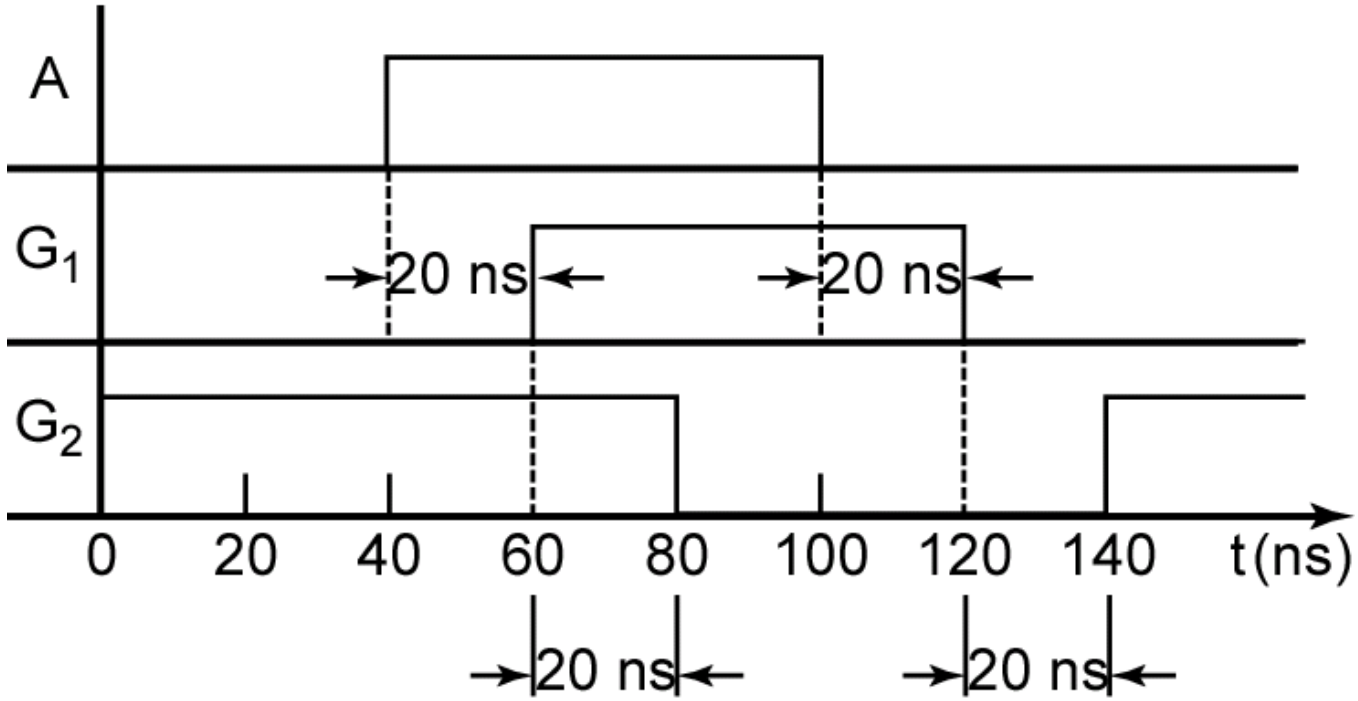
Propagation Delay in an Inverter



8.3 Gate Delays and Timing Diagrams

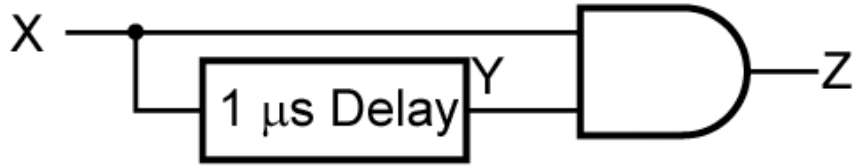
Timing Diagram for AND-NOR Circuit

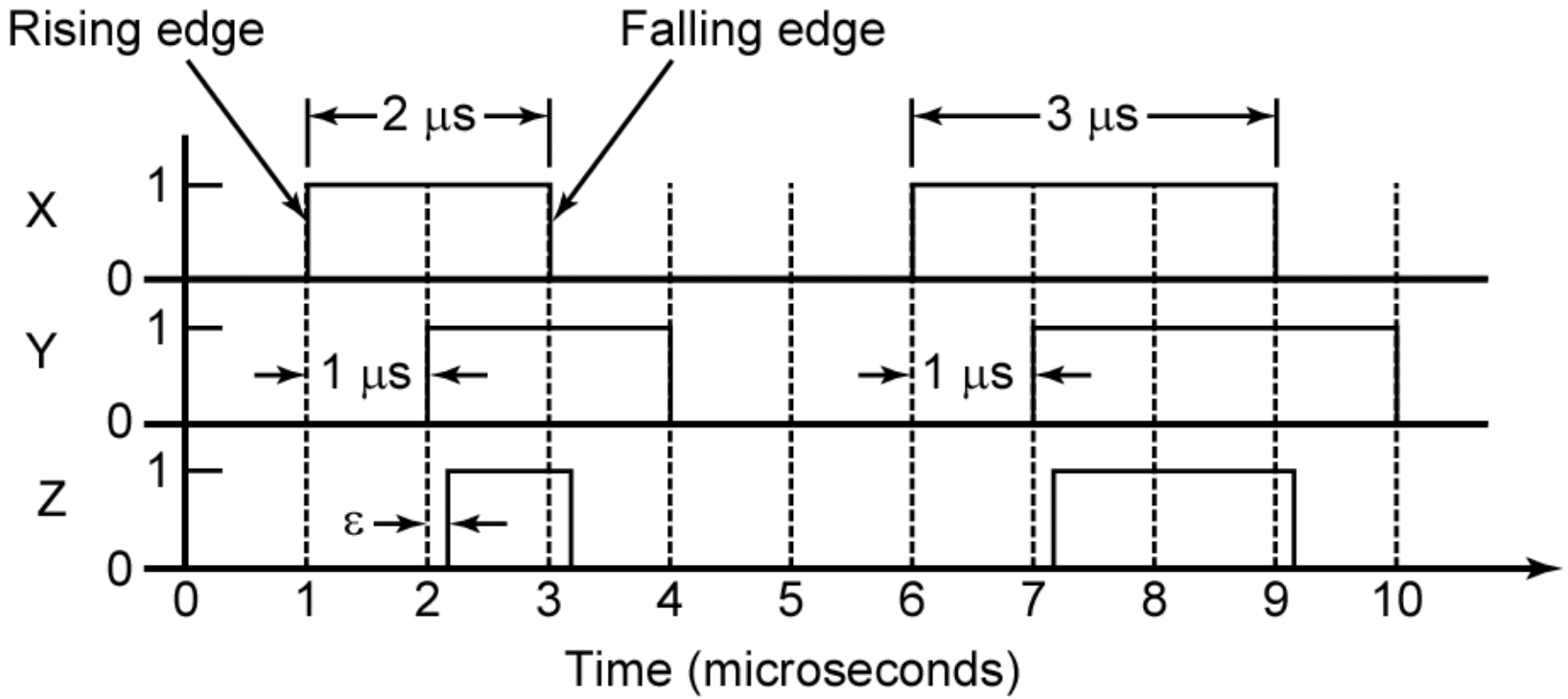




8.3 Gate Delays and Timing Diagrams

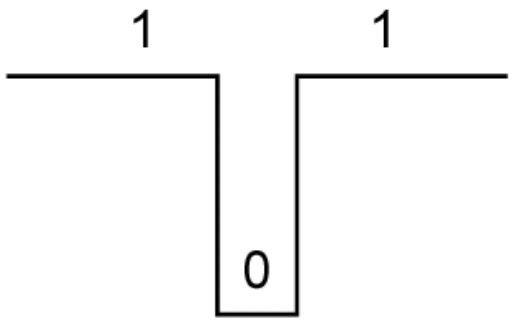
Timing Diagram for Circuit with Delay



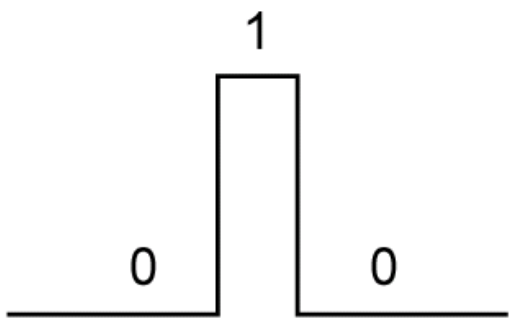


8.4 Hazards in Combinational Logic

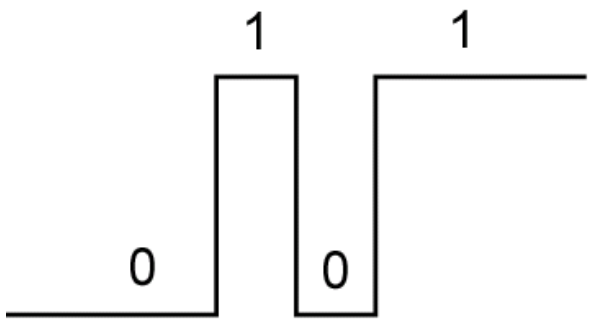
Types of Hazards

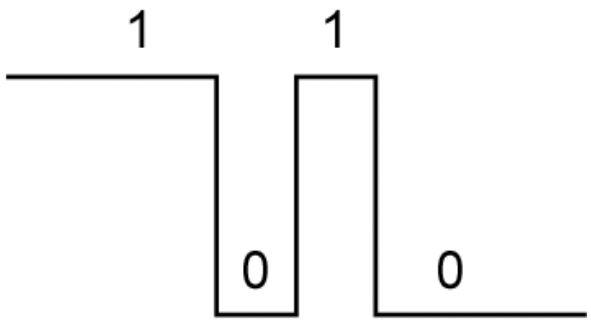


(a) Static 1-hazard



(b) Static 0-hazard



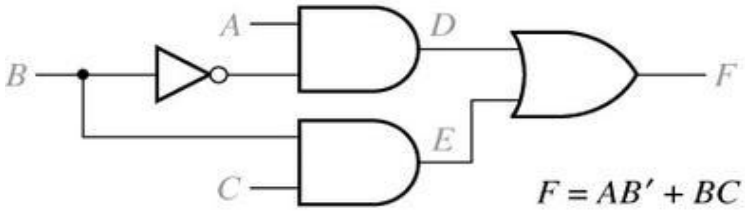


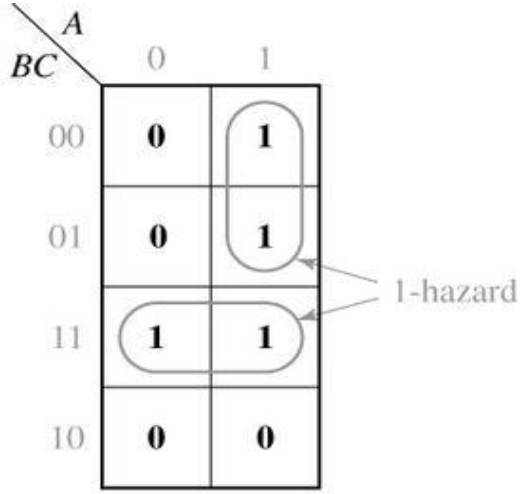
(c) Dynamic hazards

8.4 Hazards in Combinational Logic

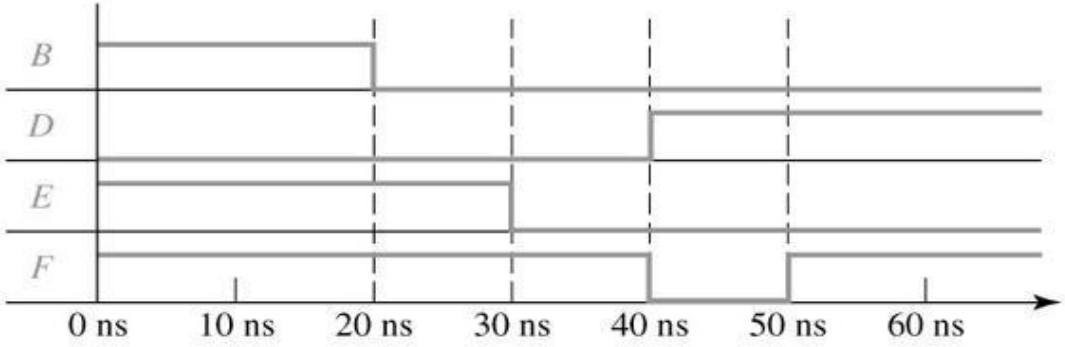
Detection of a 1-Hazard

A=1,C=1,delay=10ns





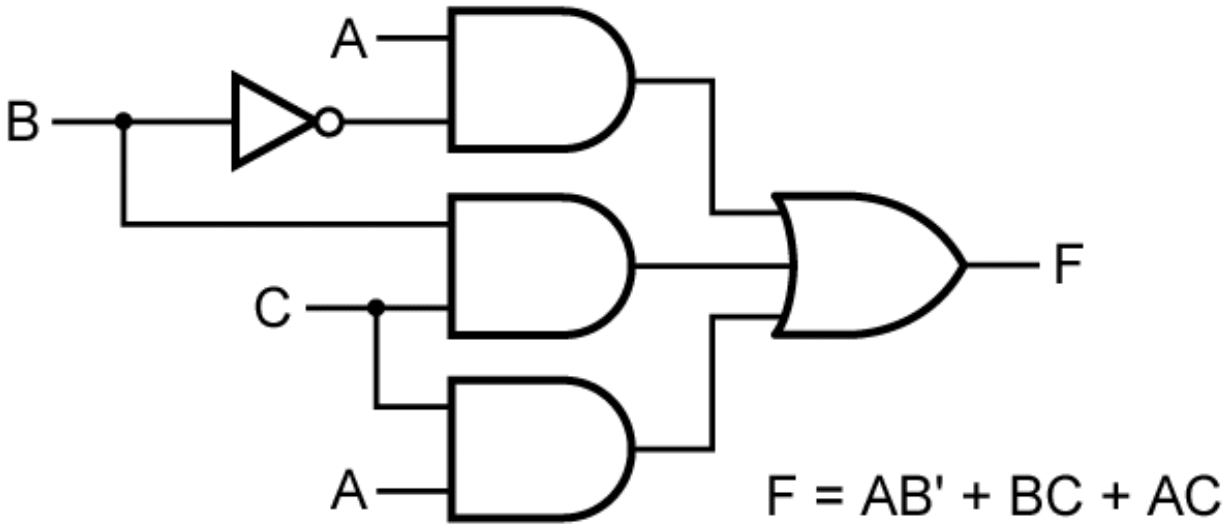
(a) Circuit with a static 1-hazard

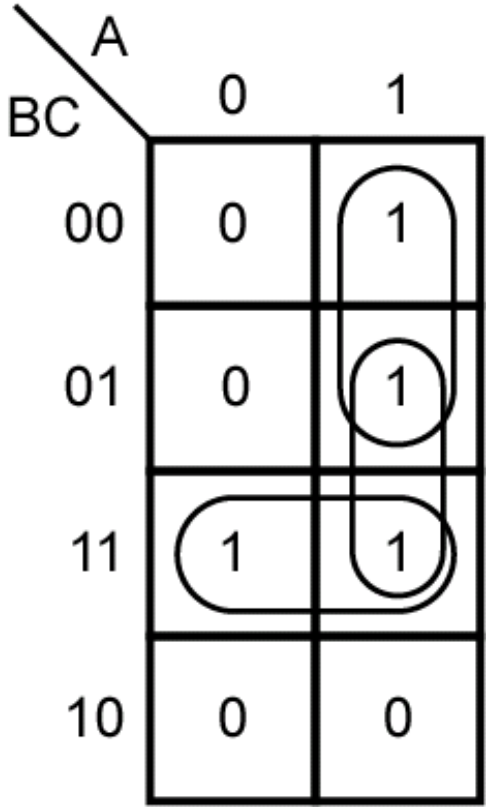


(b) Timing chart

8.4 Hazards in Combinational Logic

Circuit with Hazard Removed





8.4 Hazards in Combinational Logic

Detection of a Static 0-Hazard

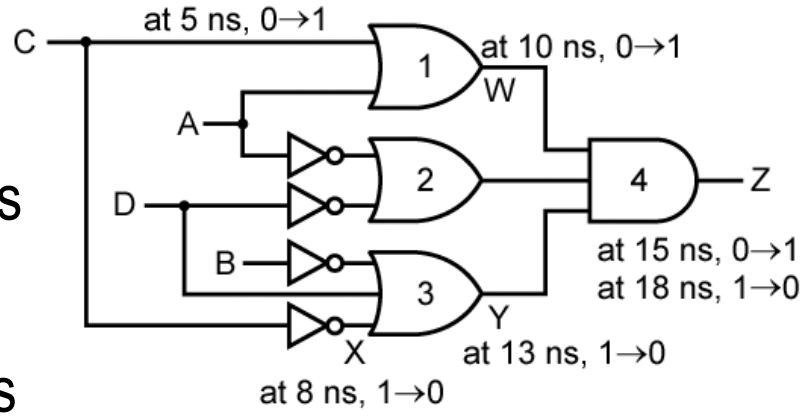
$$F = (A+C)(A'+D')(B'+C'+D)$$

A=0,B=1,

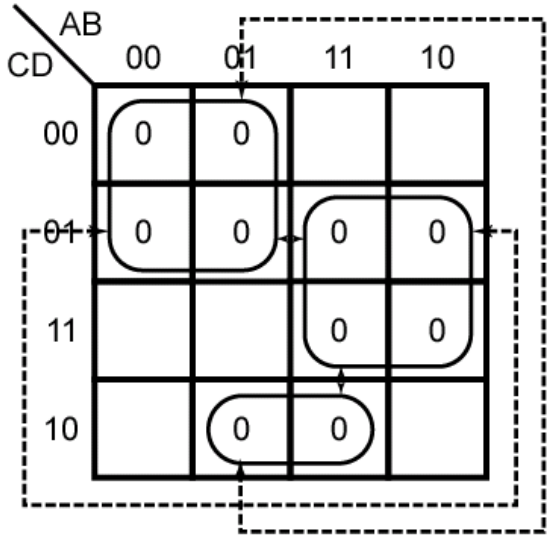
D=0

Inverter 3ns delay

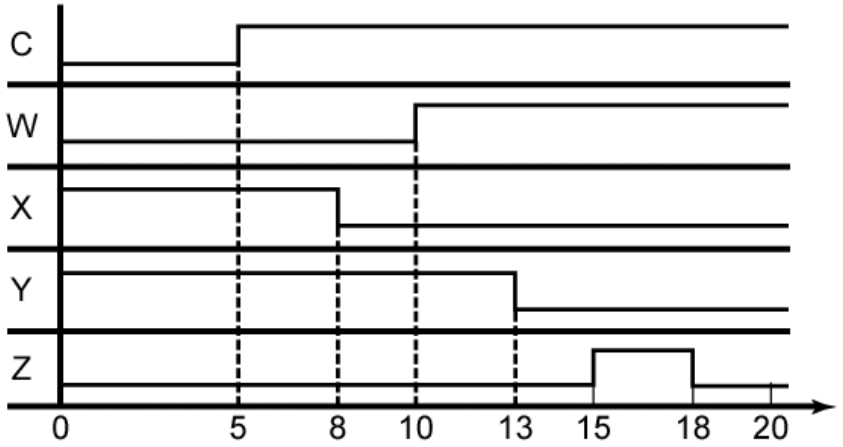
OtherGates 5ns delay



(a) Circuit with a static 0-hazard



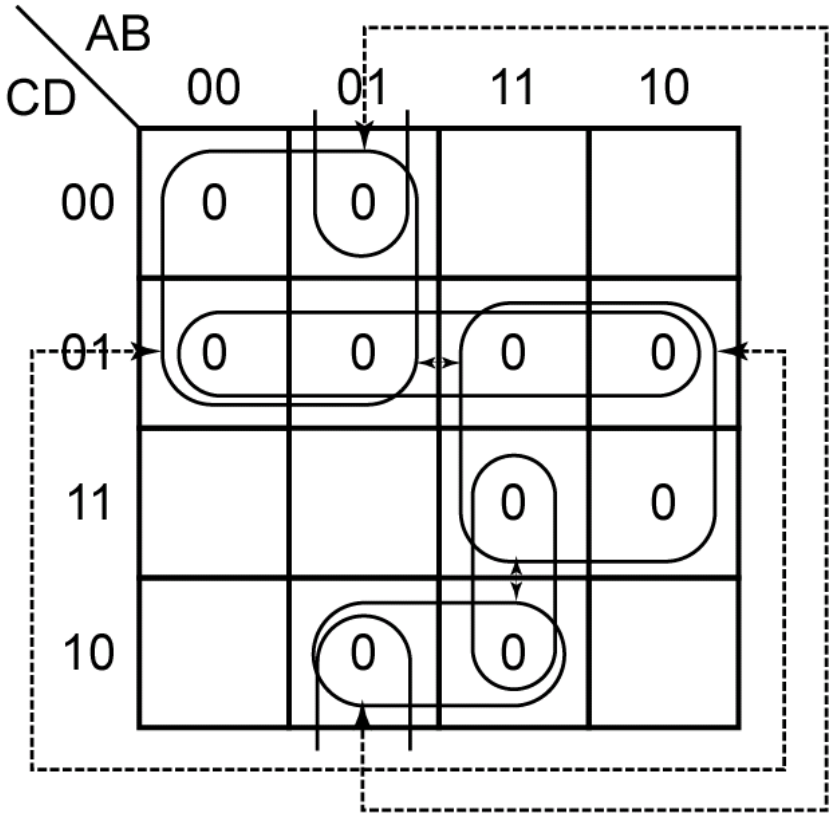
(b) Karnaugh map for circuit of (a)



(c) Timing diagram illustrating 0-hazard of (a)

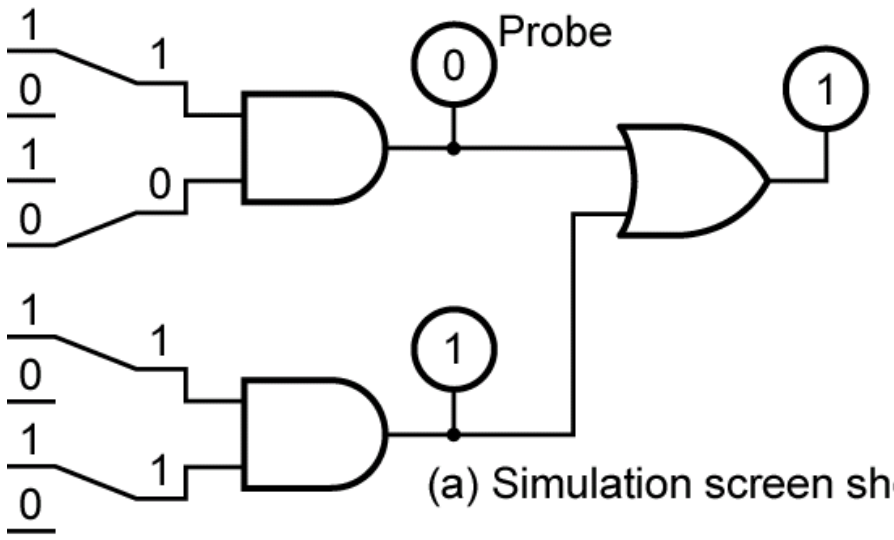
8.4 Hazards in Combinational Logic

Karnaugh Map Removing Hazards

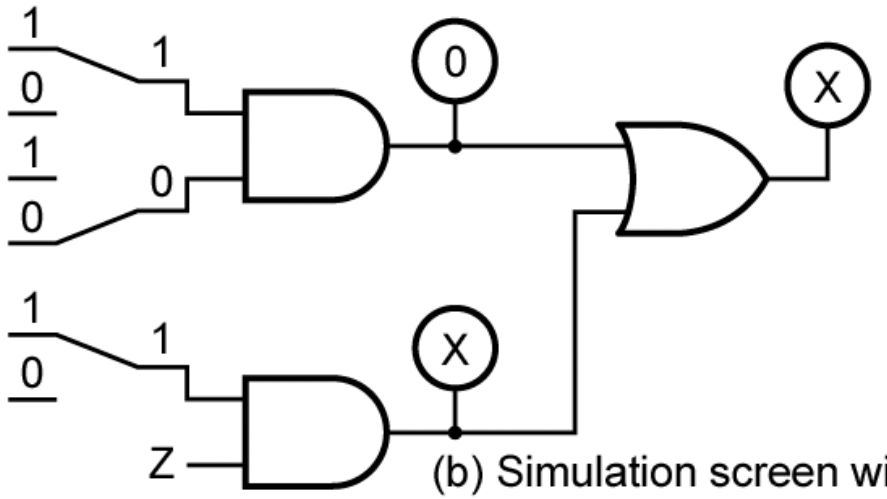


$$F = (A+C)(A'+D')(B'+C'+D)(C+D')(A+B'+D)(A'+B'+C')$$

8.5 Simulation and Testing of Logic Circuit



(a) Simulation screen showing switches



(b) Simulation screen with missing gate input

8.5 Simulation and Testing of Logic Circuit

And and OR Functions for Four-Valued Simulation

•	0	1	X	Z
0	0	0	0	0
1	0	1	X	X
X	0	X	X	X
Z	0	X	X	X

+	0	1	X	Z
0	0	1	X	X
1	1	1	1	1
X	X	1	X	X
Z	X	1	X	X

8.5 Simulation and Testing of Logic Circuit

Logic Circuit with Incorrect Output

Example: $F = AB(C'D + CD') + A'B'(C + D)$