2011년2학기
임베디드시스템 응용(#514118)

#6. A/D Converter

한림대학교
전자공학과 이선우

한림대학교
HALLYM UNIVERSITY

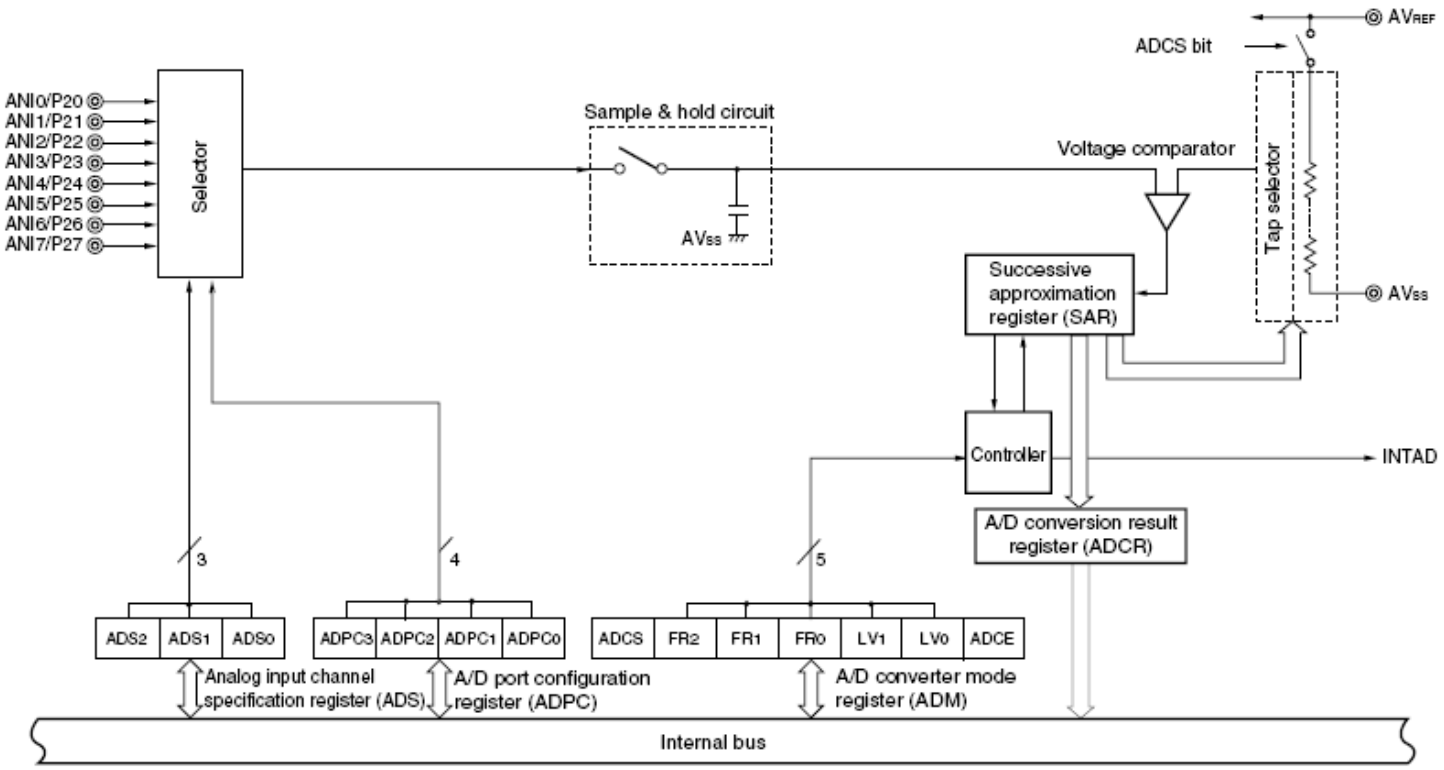
순 서

- ADC
  - Overview
  - Registers
  - Example code

Overview of ADC

- Functions
  - 8 input channels (ANI0~7)
  - 10bit resolution

Figure 13-1. Block Diagram of A/D Converter



Registers

- ADM: ADC mode reg.
- ADPC: ADC port configuration reg.
- ADS: Input channel spec. reg.
- Results → ADCR (ADCRH)

Figure 13-8. Format of Analog Input Channel Specification Register (ADS)

Address: FF29H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	0	0	0	0	0	ADS2	ADS1	ADS0

ADS2	ADS1	ADS0	Analog input channel specification
0	0	0	ANI0
0	0	1	ANI1
0	1	0	ANI2
0	1	1	ANI3
1	0	0	ANI4
1	0	1	ANI5
1	1	0	ANI6
1	1	1	ANI7

Figure 13-9. Format of A/D Port Configuration Register (ADPC)

Address: FF2FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	0	ADPC3	ADPC2	ADPC1	ADPC0

ADPC3	ADPC2	ADPC1	ADPC0	Analog input (A)/digital I/O (D) switching							
				ANI7/P27	ANI6/P26	ANI5/P25	ANI4/P24	ANI3/P23	ANI2/P22	ANI1/P21	ANI0/P20
0	0	0	0	A	A	A	A	A	A	A	A
0	0	0	1	A	A	A	A	A	A	A	D
0	0	1	0	A	A	A	A	A	A	D	D
0	0	1	1	A	A	A	A	A	D	D	D
0	1	0	0	A	A	A	A	D	D	D	D
0	1	0	1	A	A	A	D	D	D	D	D
0	1	1	0	A	A	D	D	D	D	D	D
0	1	1	1	A	D	D	D	D	D	D	D
1	0	0	0	D	D	D	D	D	D	D	D
Other than above				Setting prohibited							

ADM

Figure 13-3. Format of A/D Converter Mode Register (ADM)

Address: FF28H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	<0>
ADM	ADCS	0	FR2 Note 1	FR1 Note 1	FR0 Note 1	LV1 Note 1	LV0 Note 1	ADCE

Table 13-2. A/D Conversion Time Selection

(1) 2.7 V ≤ AVREF ≤ 5.5 V

A/D Converter Mode Register (ADM)					Conversion Time Selection				Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{PRS} = 2 MHz	f_{PRS} = 10 MHz	f_{PRS} = 20 MHz Note	
0	0	0	0	0	264/f_{PRS}	Setting prohibited	26.4 μs	13.2 μs Note	f_{PRS}/12
0	0	1	0	0	176/f_{PRS}		17.6 μs	8.8 μs Note	f_{PRS}/8
0	1	0	0	0	132/f_{PRS}		13.2 μs	6.6 μs Note	f_{PRS}/6
0	1	1	0	0	88/f_{PRS}		8.8 μs Note	Setting prohibited	f_{PRS}/4
1	0	0	0	0	66/f_{PRS}	33.0 μs	6.6 μs Note		f_{PRS}/3
1	0	1	0	0	44/f_{PRS}	22.0 μs	Setting prohibited		f_{PRS}/2
Other than above					Setting prohibited				

Note This can be set only when 4.0 V ≤ AVREF ≤ 5.5 V.

(2) 2.3 V ≤ AVREF < 2.7 V

A/D Converter Mode Register (ADM)					Conversion Time Selection			Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	
0	0	0	0	1	480/f_{PRS}	Setting prohibited	Setting prohibited	f_{PRS}/12
0	0	1	0	1	320/f_{PRS}		64.0 μs	f_{PRS}/8
0	1	0	0	1	240/f_{PRS}		48.0 μs	f_{PRS}/6
0	1	1	0	1	160/f_{PRS}		32.0 μs	f_{PRS}/4
1	0	0	0	1	120/f_{PRS}	60.0 μs	Setting prohibited	f_{PRS}/3
1	0	1	0	1	80/f_{PRS}	40.0 μs	Setting prohibited	f_{PRS}/2
Other than above					Setting prohibited			

Cautions 1. Set the conversion times with the following conditions.

- **4.0 V ≤ AVREF ≤ 5.5 V: f_{AD} = 0.6 to 3.6 MHz**
- **2.7 V ≤ AVREF < 4.0 V: f_{AD} = 0.6 to 1.8 MHz**
- **2.3 V ≤ AVREF < 2.7 V: f_{AD} = 0.6 to 1.48 MHz**

Figure 13-4. Timing Chart When Comparator Is Used

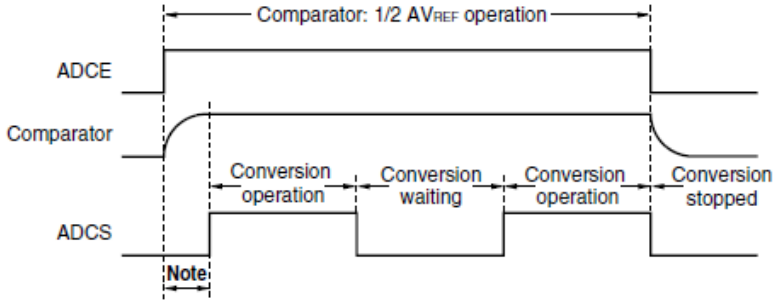
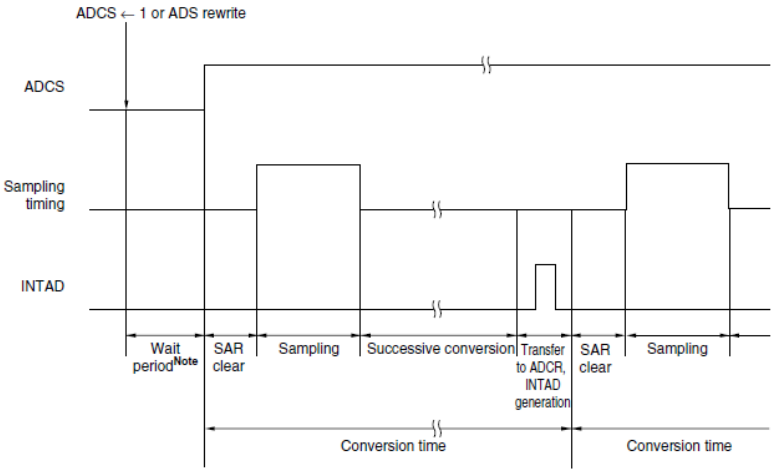


Figure 13-5. A/D Converter Sampling and A/D Conversion Timing



한림대학교 HALLYM UNIVERSITY

Conversion results

$$SAR = INT\left(\frac{V_{AIN}}{AV_{REF}} \times 1024 + 0.5\right)$$

$$ADCR = SAR \times 64$$

where, INT( ): Function which returns integer part of value in parentheses

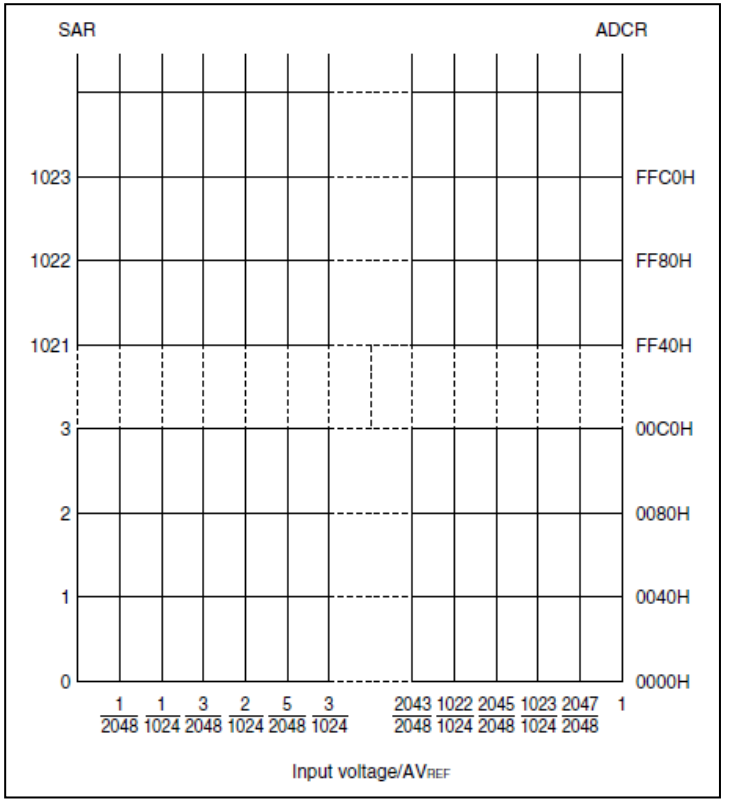
- V_{AIN}: Analog input voltage
- AV_{REF}: AV_{REF} pin voltage
- ADCR: A/D conversion result register (ADCR) value
- SAR: Successive approximation register

Figure 13-6. Format of 10-Bit A/D Conversion Result Register (ADCR)

Address: FF08H, FF09H After reset: 0000H R

Symbol	FF09H								FF08H							
ADCR											0	0	0	0	0	0

ADCRH



- Operation
  - 변환 중에 ADM에 값을 쓰면 현재 작업을 중지하고 다시 변환 시작.
  - 변환 중에 ADCS=0을 쓰면 변환 중지.
  - Fig. 13-13 참조.

How to read ADC characteristics

- Resolution
  - 디지털 출력 비트 당 애널로그 입력 전압 값
  - 1LSB=1/2^{10}=1/1024=0.098%FSR(Full Scale Range)
- Overall error
  - 실제 측정값과 이론값과의 최대 오차 값을 말함.
  - Zero-scale error, full-scale error, integral linearity error, differential linearity error 등의 조합에 의한 에러를 통칭하는 용어.
- Quantization error
  - 양자화에 따른 필연적인 오차. ➔ ±1/2LSB

How to read ADC characteristics

Figure 13-16. Zero-Scale Error

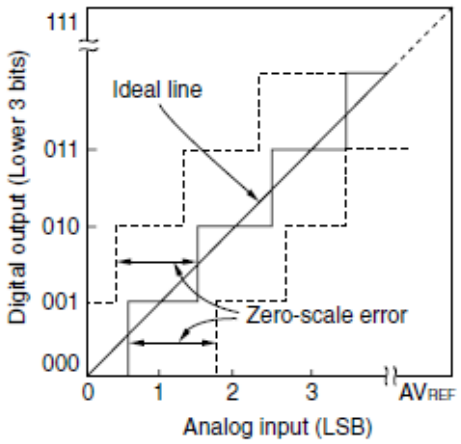


Figure 13-17. Full-Scale Error

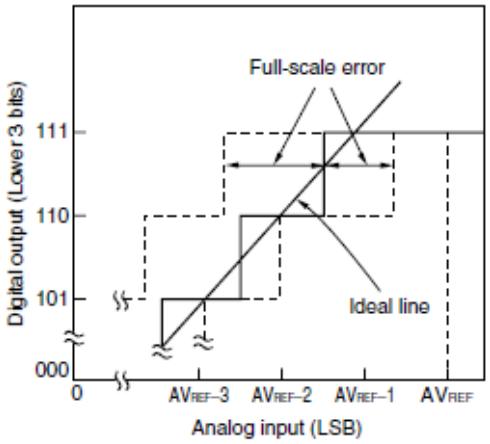


Figure 13-18. Integral Linearity Error

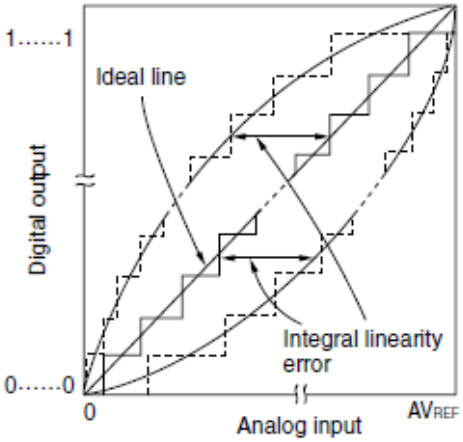
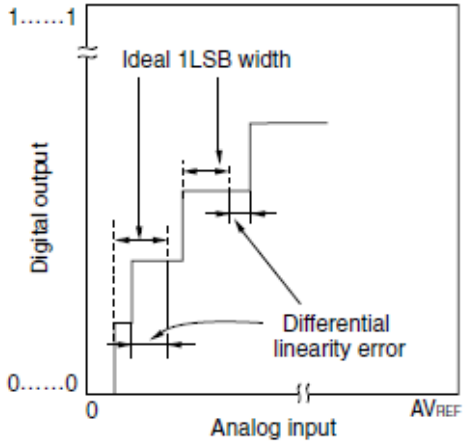


Figure 13-19. Differential Linearity Error



한림대학교 HALLYM UNIVERSITY

Code for ADC

```
__interrupt void adisr(void)
{
        uint16_t res;

        res = (ADCR>>6);
}
void main(void)
{

        //setup for ADC related regs.
        ADCE = 1;
        ADPC = 0x03;        //enable ANI0~ANI2
        ADM = 0x01;         //f=20MHz, 13.2us for conversion
        ADS = 2;            //ANI2 ch. selection
        ADMK = 0;           //enable irq.
        EI();

        while(1) {
                ADCS = 1; //start conversion
                delay(1000);
        }
}
```

ANI2에 연결된 입력 전압을 ADC하는 작업