2011년2학기
임베디드시스템 응용(#514118)

#7. Serial communication: UART

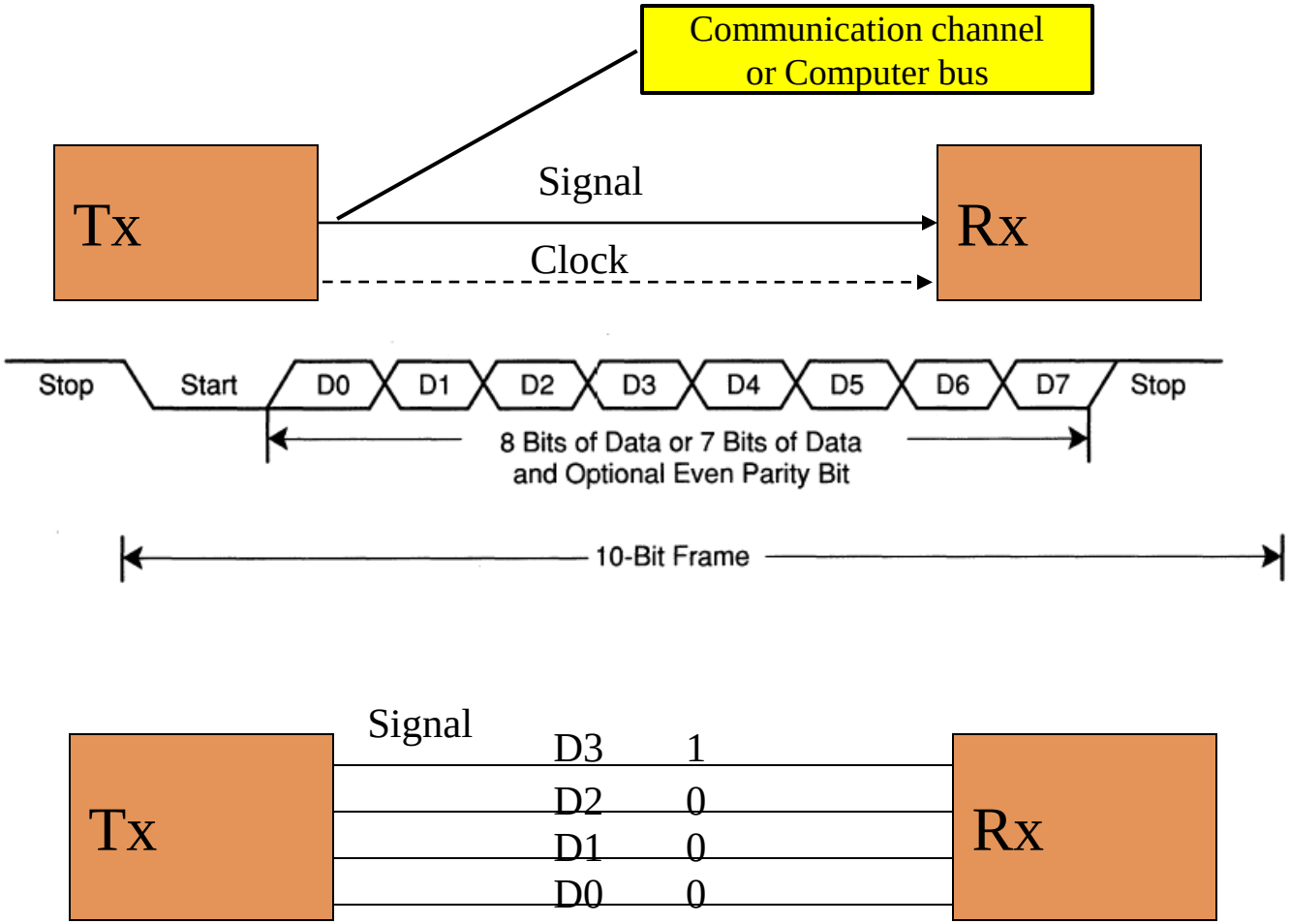
한림대학교
전자공학과 이선우

한림대학교
HALLYM UNIVERSITY

순 서

- Serial communication review
- UART0 (Ch.14)
  - Overview
  - Registers
  - Example code

Parallel vs. Serial



Examples of serial communications

- http://en.wikipedia.org/wiki/Serial_communication
  - Morse code telegraphy
  - **RS-232 (low-speed, implemented by serial ports) ***
  - RS-423
  - RS-485
  - **I^2C ***
  - **Serial Peripheral Interface Bus (SPI) ***
  - Universal Serial Bus (moderate-speed, for connecting peripherals to computers)
  - FireWire
  - Ethernet
  - Fibre Channel (high-speed, for connecting computers to mass storage devices)
  - InfiniBand (very high speed, broadly comparable in scope to PCI)
  - MIDI control of electronic musical instruments
  - DMX512 control of theatrical lighting
  - SDI-12 industrial sensor protocol
  - Serial Attached SCSI
  - Serial ATA

한림대학교 HALLYM UNIVERSITY
senu@hallym.ac.kr

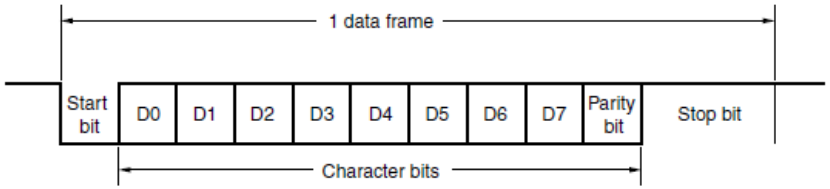
Asynchronous vs. Synchronous

- Asynchronous (비동기) 통신
  - 송신자와 수신자가 전송 이전에 동기화 필요 없음. 동기를 위한 별도 신호 필요 없음.
  - 대신 송/수신자는 반드시 동일한 클럭 주파수를 알아야 하고, 내장된 동기 신호 (start/stop bit 등) 존재해야 함
  - 항상 전송할 정보를 갖지 않는 장치, 예로 키보드, 마우스 등에 적합
  - 대표적인 표준안: RS-232C, USB 등
- Synchronous (동기) 통신
  - 비동기와 같이 데이터 전송선 이 외에 별도의 동기를 위한 신호선 (클럭 signal) 필요
  - 주요 장점: 수신자가 여러 클럭 속도에 대응 가능
  - 표준안: I^2C (필립스), SPI(Motorola) 등

78K0/KF2 Serial Interface

- Serial interfaces
  - UART supporting LIN-bus 1 channel (UART6)
  - 3-wire serial I/O/UART 1 channel (UART0/CSI10)
  - 3-wire serial I/O 1 channel (CSI11)
  - 3-wire serial I/O w auto. Tx/Rx 1 channel (CSIA0)
  - I^2C bus 1 channel (IIC0)

Figure 14-6. Format of Normal UART Transmit/Receive Data

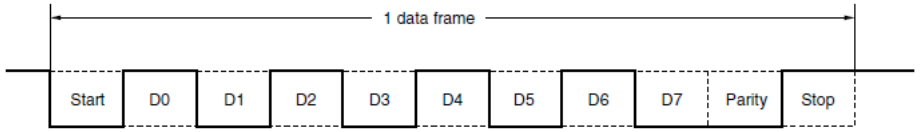


One data frame consists of the following bits.

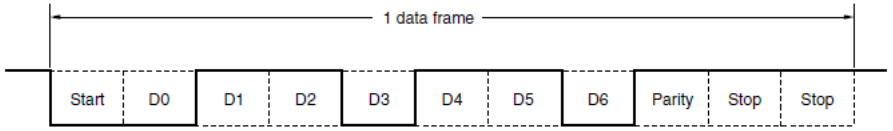
- Start bit ... 1 bit
- Character bits ... 7 or 8 bits (LSB first)
- Parity bit ... Even parity, odd parity, 0 parity, or no parity
- Stop bit ... 1 or 2 bits

Figure 14-7. Example of Normal UART Transmit/Receive Data Waveform

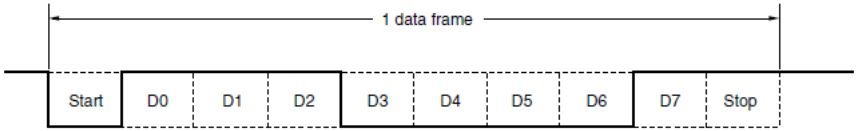
1. Data length: 8 bits, Parity: Even parity, Stop bit: 1 bit, Communication data: 55H



2. Data length: 7 bits, Parity: Odd parity, Stop bit: 2 bits, Communication data: 36H



3. Data length: 8 bits, Parity: None, Stop bit: 1 bit, Communication data: 87H



한림대학교 HALLYM UNIVERSITY

UART0 (Ch.14)

- Overview
  - Maximum transfer rate: 625kbps
  - TxD0, RxD0
  - Data length :7,8bit 선택가능
  - Full-duplex 동작 가능
  - LSB-first 통신 고정
- Configuration
  - Registers
    - Receive buffer reg.0 (RXB0), Rec./Tra. shift reg. RXS0, TXS0
  - Control reg.
    - ASIM0, ASIS0, BRGC0, PM1, P1

Operations

- Stop mode
  - UART 기능을 사용하지 않을 때 사용. 전력 소비 절약 효과. P11, P10 port 기능 사용 가능.
  - Setting
    - ASIM0<7:POWER0><6:TXE0><5:RXE0> =0 (clear)
- UART mode
  - 설정 순서
    1. BRGC0 설정 (boad rate clock 설정)
    2. ASIM0<1~4> bit 설정 (Rx/Tx pin 설정)
    3. ASIM0<7>=1, TXE0=1, RXE0=1
    4. TXS0←data 쓰기 ➔ 데이터 전송 시작

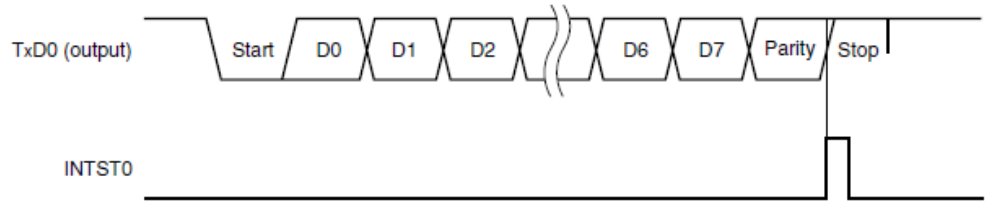
Table 14-2. Relationship Between Register Settings and Pins

POWER0	TXE0	RXE0	PM10	P10	PM11	P11	UART0 Operation	Pin Function	
								TxD0/$\overline{\text{SCK10}}$/P10	RxD0/SI10/P11
0	0	0	×Note	×Note	×Note	×Note	Stop	$\overline{\text{SCK10}}$/P10	SI10/P11
1	0	1	×Note	×Note	1	×	Reception	$\overline{\text{SCK10}}$/P10	RxD0
	1	0	0	1	×Note	×Note	Transmission	TxD0	SI10/P11
	1	1	0	1	1	×	Transmission/ reception	TxD0	RxD0

Tx/Rx IRQ Timing

Figure 14-8. Transmission Completion Interrupt Request Timing

1. Stop bit length: 1



2. Stop bit length: 2

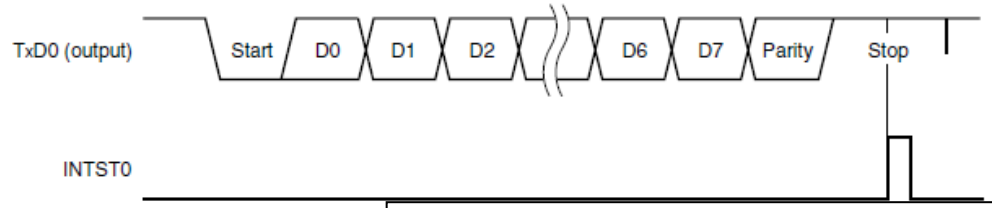
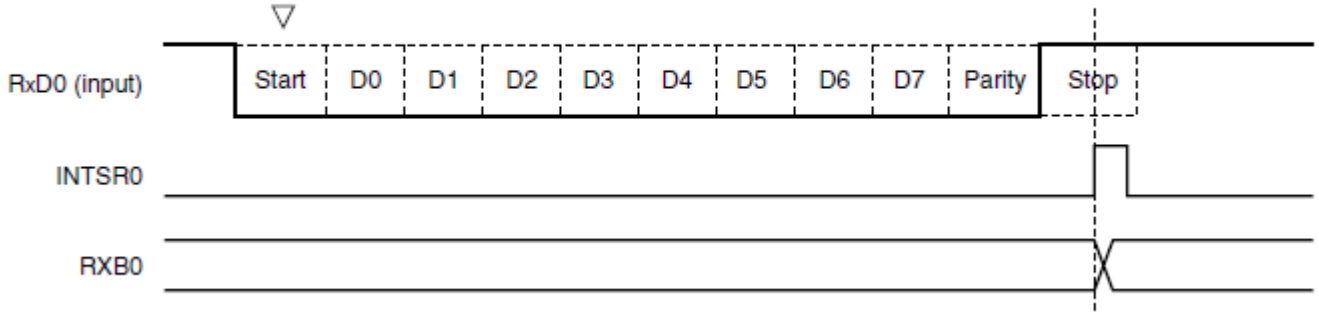


Figure 14-9. Reception Completion Interrupt Request Timing



Control registers

Figure 14-2. Format of Asynchronous Serial Interface Operation Mode Register 0 (ASIM0) (1/2)

Address: FF70H After reset: 01H R/W

Symbol	<7>	<6>	<5>	4	3	2	1	0
ASIM0	POWER0	TXE0	RXE0	PS01	PS00	CL0	SL0	1

PS01	PS00	Transmission operation	Reception operation
0	0	Does not output parity bit.	Reception without parity
0	1	Outputs 0 parity.	Reception as 0 parity[Note]
1	0	Outputs odd parity.	Judges as odd parity.
1	1	Outputs even parity.	Judges as even parity.

CL0	Specifies character length of transmit/receive data
0	Character length of data = 7 bits
1	Character length of data = 8 bits

SL0	Specifies number of stop bits of transmit data
0	Number of stop bits = 1
1	Number of stop bits = 2

PE0	Status flag indicating parity error
0	If POWER0 = 0 or RXE0 = 0, or if ASIS0 register is read.
1	If the parity of transmit data does not match the parity bit on completion of reception.

FE0	Status flag indicating framing error
0	If POWER0 = 0 or RXE0 = 0, or if ASIS0 register is read.
1	If the stop bit is not detected on completion of reception.

OVE0	Status flag indicating overrun error
0	If POWER0 = 0 and RXE0 = 0, or if ASIS0 register is read.
1	If receive data is set to the RXB0 register and the next reception operation is completed before the data is read.

Rx Errors
- Parity
- Framing
- Overrun

Figure 14-3. Format of Asynchronous Serial Interface Reception Error Status Register 0 (ASIS0)

Address: FF73H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ASIS0	0	0	0	0	0	PE0	FE0	OVE0

Baud rate generation

Figure 14-4. Format of Baud Rate Generator Control Register 0 (BRGC0)

Address: FF71H After reset: 1FH R/W

Symbol	7	6	5	4	3	2	1	0
BRGC0	TPS01	TPS00	0	MDL04	MDL03	MDL02	MDL01	MDL00

TPS01	TPS00	Base clock (f_{XCLK0}) selection				
			f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz	f_{PRS} = 20 MHz
0	0	TM50 output[Note]				
0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz
1	0	$f_{PRS}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz
1	1	$f_{PRS}/2^5$	62.5 kHz	156.25 kHz	312.5 kHz	625 kHz

MDL04	MDL03	MDL02	MDL01	MDL00	k	Selection of 5-bit counter output clock
0	0	×	×	×	×	Setting prohibited
0	1	0	0	0	8	$f_{XCLK0}/8$
0	1	0	0	1	9	$f_{XCLK0}/9$
0	1	0	1	0	10	$f_{XCLK0}/10$
•	•	•	•	•	•	•
1	1	0	1	0	26	$f_{XCLK0}/26$
1	1	0	1	1	27	$f_{XCLK0}/27$
1	1	1	0	0	28	$f_{XCLK0}/28$
1	1	1	0	1	29	$f_{XCLK0}/29$
1	1	1	1	0	30	$f_{XCLK0}/30$
1	1	1	1	1	31	$f_{XCLK0}/31$

Baud rate [bps] = $f_{XCLK0}/2*k$

Ex)

f_{XCLK0}=2.5MHz

k = 16

Baud rate=2.5M/(2*16)=78125

Error = (78125/76800 – 1)*100

= 1.725%

*설정에 따른 보드레이트는 에러 값은 표 14-5 참조할 것.

Code for UART0

```
#pragma vect INTSR0 uart0_rx
__interrupt void uart0_rx(void)
{
        unsigned char ch;
        ch = RXS0;
        if(ASIS0 & 0x07) {//check errors
           P2 |= ASIS0 & 0x07;
        else  //transmit the received char.
           TXS0 = ch;
}
void main(void)
{
        //setup for UART0
        BRGC0 = 0b10001011; //TPS=2, k=11→115200bps
        PM1.0 = 0; P1.0 = 1; //for TxD0
        PM1.1 = 1; //for RxD0
        ASIM0 = 0b11100101; //8N1
        SRMK0 = 0; //Irq. Mask flag for INTSR0
        EI();
}
```

UART0를 통해 입력된 문자를 그대로 serial로 출력하는 프로그램
* 가정: P2.2~0에 3개 LED 연결.