

2011년2학기
임베디드시스템 응용 (#514118)
#8. Serial communication 2
LIN, UART6

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순서

- ▶ UART0 (Ch.14)
 - ▶ Code correction
- ▶ Controller Area Network
- ▶ Local Interconnect Network
- ▶ UART6

Code for UART0

```
#pragma vect INTSR0 uart0_rx
__interrupt void uart0_rx(void)
{
    unsigned char ch, er;
    ch = RXB0;
    er = ASIS0; //after read to be cleared
    if(er & 0x07) { //check errors
        P2 |= er & 0x07;
    }
    else //transmit the received char.
        TXS0 = ch;
}
void main(void)
{
    //setup for UART0
    BRGC0 = 0b10001011; //TPS=2, k=11→115200bps
    PM1.0 = 0; P1.0 = 1; //for TxD0
    PM1.1 = 1; //for RxD0
    ASIM0 = 0b11100101; //8N1
    SRMK0 = 0; //Irr. Mask flag for INTSR0
    EI();
}
```

Controller-Area Network (CAN)

▶ Sources

- ▶ http://en.wikipedia.org/wiki/Controller_Area_Network
- ▶ <http://www.ni.com/can/>

▶ 정의: 자동차 내의 전자장치들끼리의 통신 규격 (standard)

▶ 역사

- ▶ 1983년 독일 Bosch사에서 차량 네트워크용으로 개발.
- ▶ 1986년 프로토콜 발표
- ▶ 1987년 인텔, 필립스사에 의해 최초 CAN-bus용 칩 개발.
- ▶ 1991년 CAN 2.0 specification 발표
- ▶ 1993년 ISO 11898로 국제 규격으로 채택

CAN Overview

▶ 배경

- ▶ 자동차에서의 ECU(electron control unit) 사용 증가. (최소 70 이상의 ECU 사용. ECM, PCM, trans., airbags, ABS, cruise control, EPS, etc.)
- ▶ 이런 모듈 사이의 정보 교환이 필요해짐 → CAN 개발 필요
- ▶ CAN-bus는 일반적인 자동 제어 시스템에서도 사용 확대
- ▶ Bosch가 특허 소유. 특허료 CAN Protocol License에 따라 지급해야 함.

▶ Applications

- ▶ 자동차, 철도, 엘리베이터 및 에스컬레이터 등 운송 시스템 등
- ▶ 항공기, 우주항공기, 자동제어 시스템 등
- ▶ 의료기기 시스템 등

CAN Overview

▶ Technology

- ▶ CAN is a multi-master broadcast serial bus standard.
- ▶ 각 노드는 메시지 송/수신 가능 (동시 불가)
- ▶ 메시지에 ID 포함
- ▶ 각 노드는 host processor, CAN controller, Transceiver로 구성됨.
- ▶ 속도(bit rate)는 40m 이하의 네트워크 길이에서 최대 1Mbit/s.

▶ Priority-based bus arbitration

- ▶ 각 노드의 ID의 숫자가 작을 수록 높은 우선 순위. 0이 1보다 높은 우선 순위 가짐. Open collector/wired/logical AND 연결 때문.

CAN Overview

▶ Physical layer

- ▶ 전기적 레벨, 신호 구조, 케이블 임피던스, 최대 보드 레이트 등 특징사항 정의
- ▶ High-speed CAN
 - ▶ 2 wire 사용, speed < 1Mbit/s
 - ▶ Another name: ISO 11898-2
- ▶ Low-speed/Fault-tolerant CAN
 - ▶ 2 wire, speed < 125kbit/s
 - ▶ Another name: fault-tolerant CAN, CAN B, ISO 11898-3
 - ▶ Main apps. : door system
- ▶ Single-wire CAN
 - ▶ Use single-wire at rates up to 33.3kbits/s.

CAN Overview

▶ Frames (packet)

- ▶ Packet: formatted block of data

- ▶ 4 types

 - ▶ Data frame: 일반 데이터 내장 프레임

 - ▶ Remote frame: 특정 노드의 전송 요청 프레임

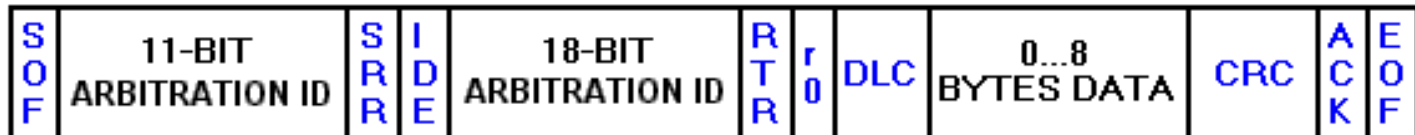
 - ▶ Error frame: 에러가 발견된 노드에 의해 발송되는 프레임

 - ▶ Overload frame

- ▶ Data frame

 - ▶ Base frame format: with 11 identifier bits

 - ▶ Extended frame format: with 29 id. bits



Local Interconnect Network (LIN)

▶ LIN-Bus

- ▶ A small and slow network as a cheap sub-network of a CAN
- ▶ Network topology
 - ▶ Broadcast serial network with 1 master and up to 12 slaves.
 - ▶ All messages are initiated by the master with at most one slave replying for a given id.
- ▶ History
 - ▶ 1990년대 유럽 5개 자동차 회사 등 개발
 - ▶ 2002.11월 LIN v1.3, 2003년9월 v2.0 발표

*source:

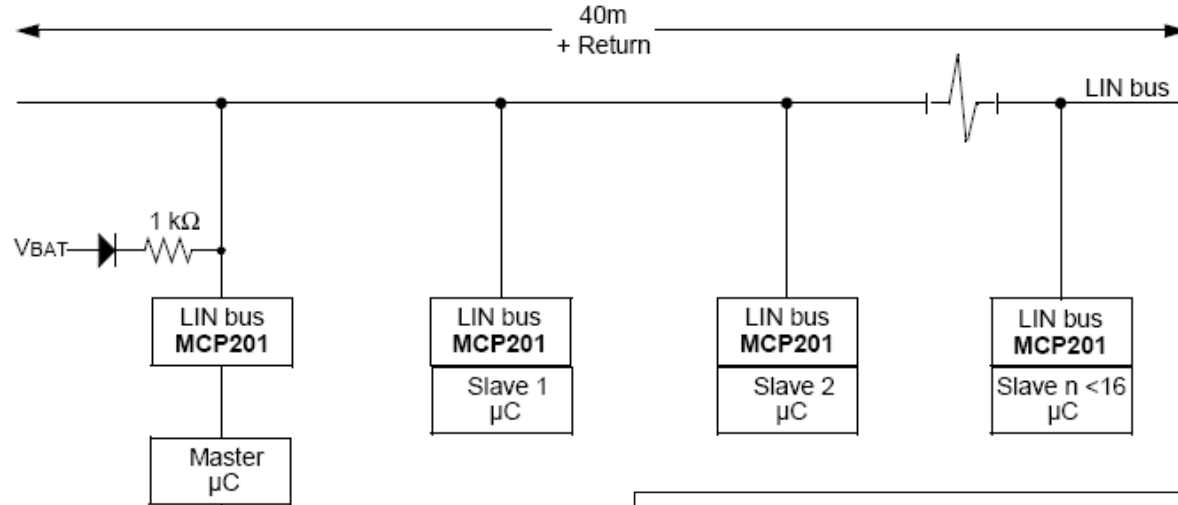
http://en.wikipedia.org/wiki/Local_Interconnect_Network#Network_topology

LIN-Bus

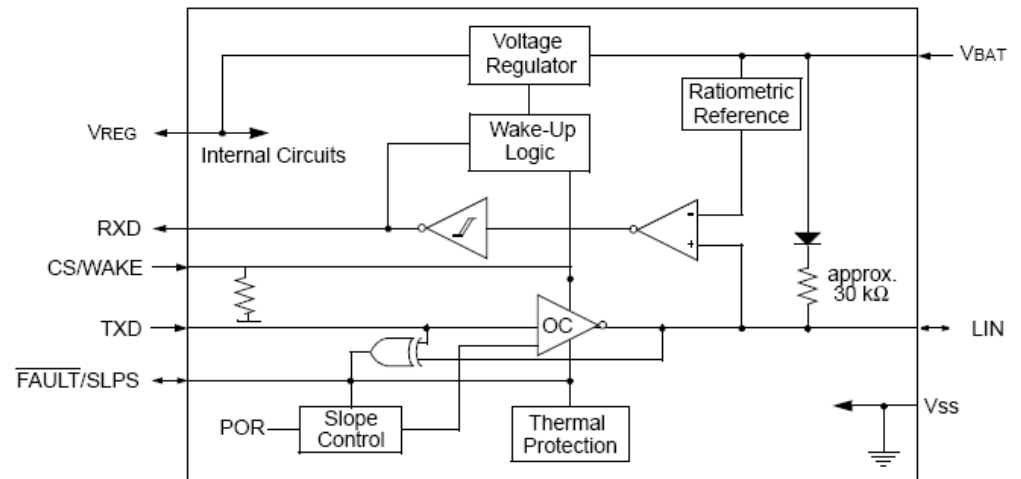
- ▶ Features of protocol
 - ▶ Single master, up to 16 slaves
 - ▶ Single wire communications up to 19.2kbit/s @ 40m bus length
 - ▶ Guaranteed latency time
 - ▶ Variable length of data frame (2/4/8 bytes)
 - ▶ Data checksum and error detection
 - ▶ Detection of defective nodes
 - ▶ Low cost silicon implementation based on standard UART/SCI hardware
 - ▶ Operating voltage of 12V

LIN-Bus

▶ LIN network configuration

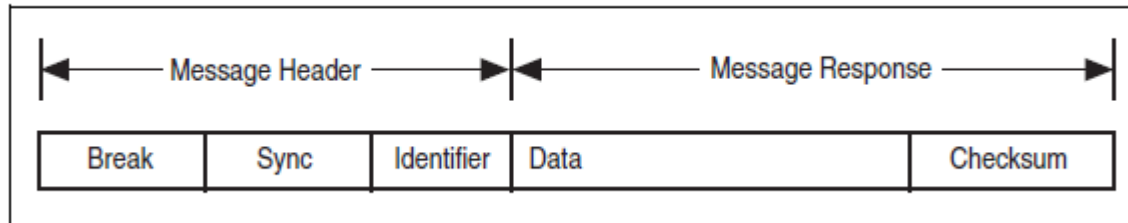


▶ LIN transceiver



LIN-Bus

▶ Frame format



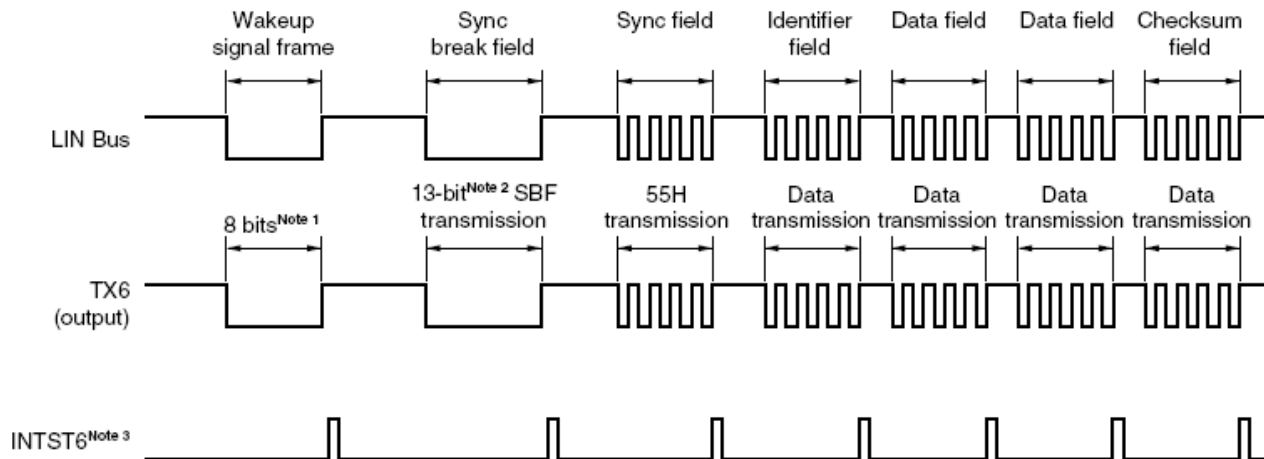
- ▶ Break: 13 dominant bits, serve as a start-of-frame(SOF)
- ▶ Sync:0x55, slave device들이 자동으로 baud rate을 감지하게 하기 위함.
- ▶ ID:응답하기 원하는 노드 지정. 0~59;data frame, 60,61;carry/diagnostic data, 62;user-defined extensions, 63;future protocol enhancement.

UART6

▶ Features

- ▶ Maximum transfer rate: 625kbps
- ▶ Data length: 7 or 8bits
- ▶ 8-bit baud rate generator
- ▶ Full duplex operation
- ▶ MSB- or LSB-first comm. Selectable
- ▶ Sync Break Field (SBF) transmission from 13 to 20 bits

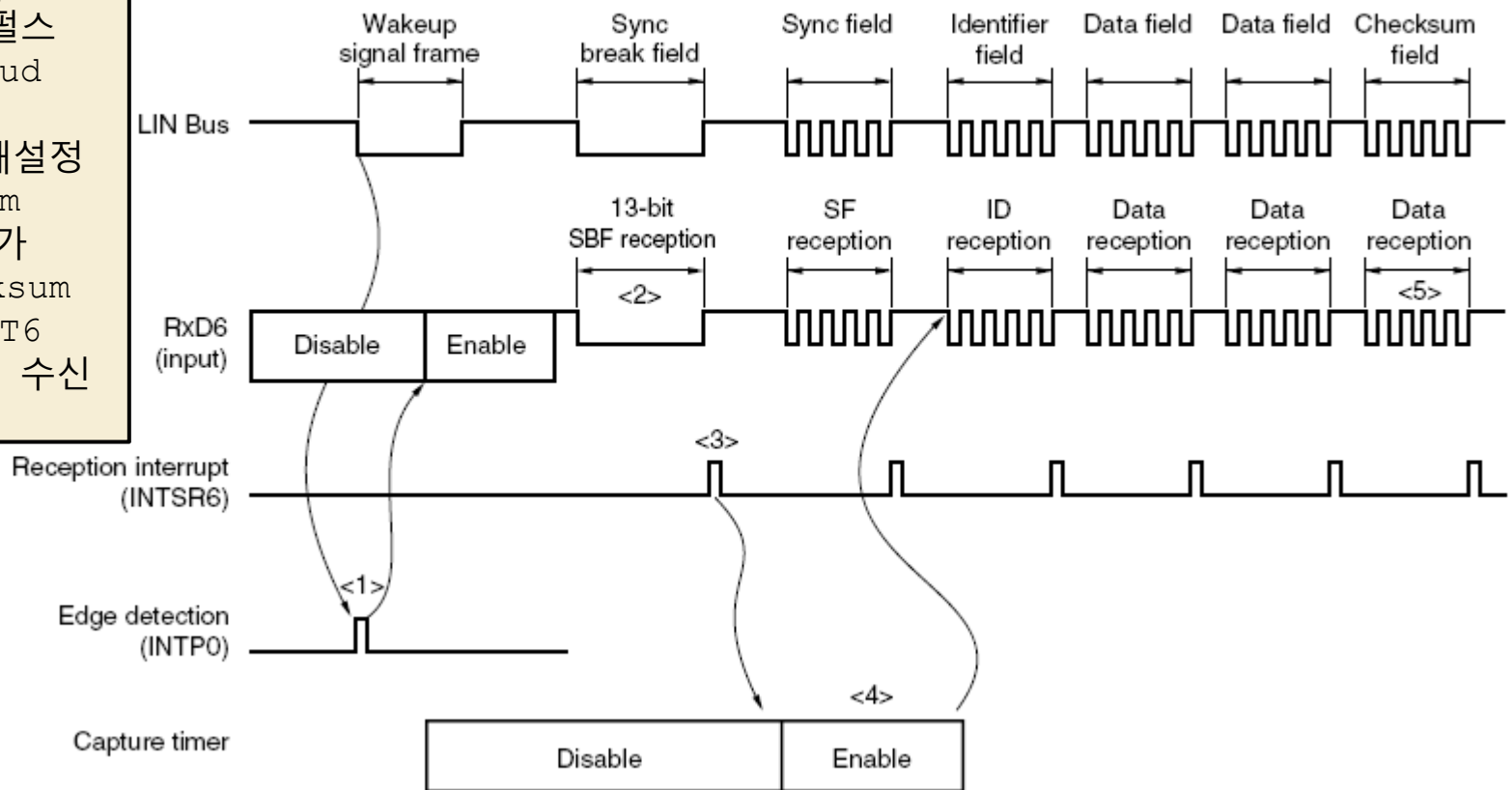
Figure 15-1. LIN Transmission Operation



UART6: LIN reception operation

<1>UART6활성화 &
 SBF 수신 설정.
 <3>SBF 수신
 완료되면 INTSR6
 발생, 타이머00
 활성화시켜 펄스
 폭 측정, baud
 rate 결정
 <4>BRGC6 재설정
 <5>Checksum
 데이터는 SW가
 검사. checksum
 수신 후 UART6
 초기화, SBF 수신
 재설정.

Figure 15-2. LIN Reception Operation



Configuration 비교 UART0/6

▶ 다른 점

- ▶ 4개 reg. 추가: TXB6, ASIF6, CKSR6, ASICL6

Table 14-1. Configuration of Serial Interface UART0

Item	Configuration
Registers	Receive buffer register 0 (RXB0) Receive shift register 0 (RXS0) Transmit shift register 0 (TXS0)
Control registers	Asynchronous serial interface operation mode register 0 (ASIM0) Asynchronous serial interface reception error status register 0 (ASIS0) Baud rate generator control register 0 (BRGC0) Port mode register 1 (PM1) Port register 1 (P1)

Table 15-1. Configuration of Serial Interface UART6

Item	Configuration
Registers	Receive buffer register 6 (RXB6) Receive shift register 6 (RXS6) Transmit buffer register 6 (TXB6) Transmit shift register 6 (TXS6)
Control registers	Asynchronous serial interface operation mode register 6 (ASIM6) Asynchronous serial interface reception error status register 6 (ASIS6) Asynchronous serial interface transmission status register 6 (ASIF6) Clock selection register 6 (CKSR6) Baud rate generator control register 6 (BRGC6) Asynchronous serial interface control register 6 (ASICL6) Input switch control register (ISC) Port mode register 1 (PM1) Port register 1 (P1)

Control registers for baud rate

- ▶ Clock selection reg.6 (CKSR6)
- ▶ Baud rate generator control reg.6(BRGC6)

Figure 15-8. Format of Clock Selection Register 6 (CKSR6)

56H After reset: 00H R/W

7	6	5	4	3	2	1	0
0	0	0	0	TPS63	TPS62	TPS61	TPS60

TPS63	TPS62	TPS61	TPS60		Base clock (f _{CLK6}) selection			
					f _{PRS} = 2 MHz	f _{PRS} = 5 MHz	f _{PRS} = 10 MHz	f _{PRS} = 20 MHz
0	0	0	0	f _{PRS}	2 MHz	5 MHz	10 MHz	20 MHz
0	0	0	1	f _{PRS} /2	1 MHz	2.5 MHz	5 MHz	10 MHz
0	0	1	0	f _{PRS} /2 ²	500 kHz	1.25 MHz	2.5 MHz	5 MHz
0	0	1	1	f _{PRS} /2 ³	250 kHz	625 kHz	1.25 MHz	2.5 MHz
0	1	0	0	f _{PRS} /2 ⁴	125 kHz	312.5 kHz	625 kHz	1.25 MHz
0	1	0	1	f _{PRS} /2 ⁵	62.5 kHz	156.25 kHz	312.5 kHz	625 kHz
0	1	1	0	f _{PRS} /2 ⁶	31.25 kHz	78.13 kHz	156.25 kHz	312.5 kHz
0	1	1	1	f _{PRS} /2 ⁷	15.625 kHz	39.06 kHz	78.13 kHz	156.25 kHz
1	0	0	0	f _{PRS} /2 ⁸	7.813 kHz	19.53 kHz	39.06 kHz	78.13 kHz
1	0	0	1	f _{PRS} /2 ⁹	3.906 kHz	9.77 kHz	19.53 kHz	39.06 kHz
1	0	1	0	f _{PRS} /2 ¹⁰	1.953 kHz	4.88 kHz	9.77 kHz	19.53 kHz
1	0	1	1	TM50 output ^{Note}				
Other than above					Setting prohibited			

Figure 15-9. Format of Baud Rate Generator Control Register 6 (BRGC6)

F57H After reset: FFH R/W

7	6	5	4	3	2	1	0
MDL67	MDL66	MDL65	MDL64	MDL63	MDL62	MDL61	MDL60

MDL67	MDL66	MDL65	MDL64	MDL63	MDL62	MDL61	MDL60	k	Output clock selection of 8-bit counter
0	0	0	0	0	0	×	×	×	Setting prohibited
0	0	0	0	0	1	0	0	4	f _{CLK6} /4
0	0	0	0	0	1	0	1	5	f _{CLK6} /5
0	0	0	0	0	1	1	0	6	f _{CLK6} /6
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	0	0	252	f _{CLK6} /252
1	1	1	1	1	1	0	1	253	f _{CLK6} /253
1	1	1	1	1	1	1	0	254	f _{CLK6} /254
1	1	1	1	1	1	1	1	255	f _{CLK6} /255

Async. serial interface control (ASICL6)

Figure 15-10. Format of Asynchronous Serial Interface Control Register 6 (ASICL6) (1/2)

Address: FF58H After reset: 16H R/W^{Note}

Symbol	<7>	<6>	5	4	3	2	1	0
ASICL6	SBRF6	SBRT6	SBTT6	SBL62	SBL61	SBL60	DIR6	TXDLV6

SBRF6	SBF reception status flag
0	If POWER6 = 0 and RXE6 = 0 or if SBF reception has been completed correctly
1	SBF reception in progress

Figure 15-10. Format of Asynchronous Serial Interface Control Register 6 (ASICL6) (2/2)

SBRT6	SBF reception trigger
0	-
1	SBF reception trigger

SBTT6	SBF transmission trigger
0	-
1	SBF transmission trigger

SBL62	SBL61	SBL60	SBF transmission output width control
1	0	1	SBF is output with 13-bit length.
1	1	0	SBF is output with 14-bit length.
1	1	1	SBF is output with 15-bit length.
0	0	0	SBF is output with 16-bit length.
0	0	1	SBF is output with 17-bit length.
0	1	0	SBF is output with 18-bit length.
0	1	1	SBF is output with 19-bit length.
1	0	0	SBF is output with 20-bit length.

DIR6	First-bit specification
0	MSB
1	LSB

TXDLV6	Enables/disables inverting TxD6 output
0	Normal output of TxD6
1	Inverted output of TxD6

Another registers

▶ Input switch control reg. (ISC)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ISC1	ISC0

ISC1	TI000 input source selection
0	TI000 (P00)
1	RxD6 (P14)

ISC0	INTP0 input source selection
0	INTP0 (P120)
1	RxD6 (P14)

▶ PM1

- ▶ PM13=0, P13=1 for P13/TxD6 pin
- ▶ PM14=1 for P14/RxD6 pin

Timing of continuous transmission

Figure 15-17. Timing of Starting Continuous Transmission

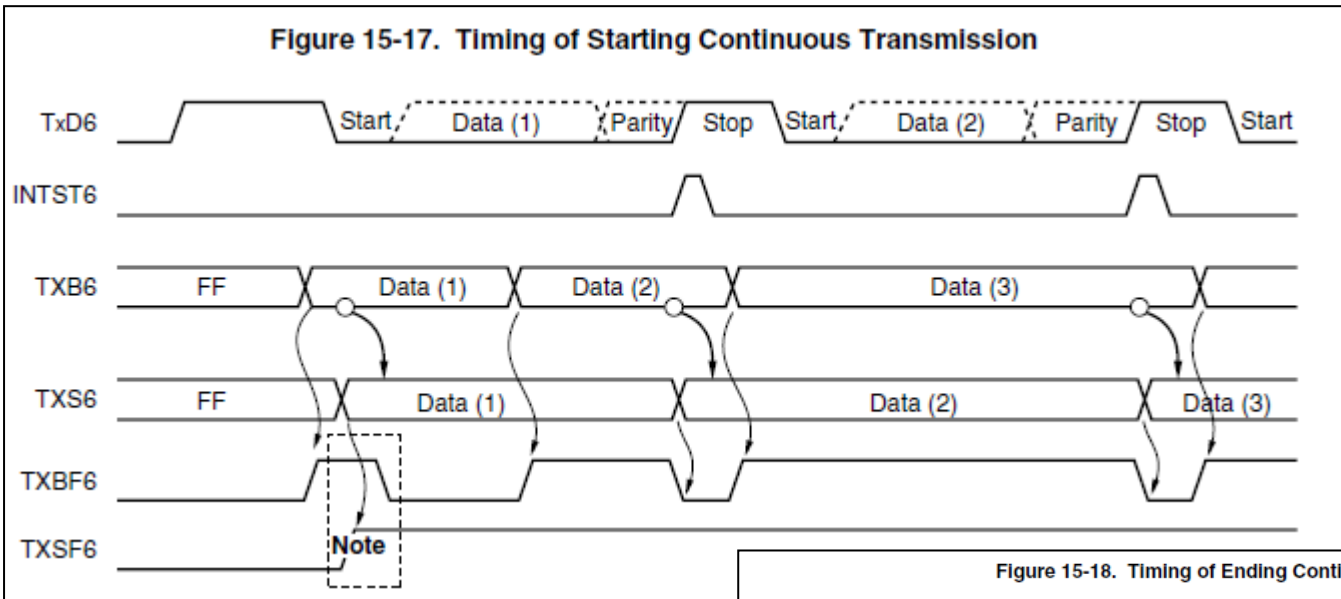
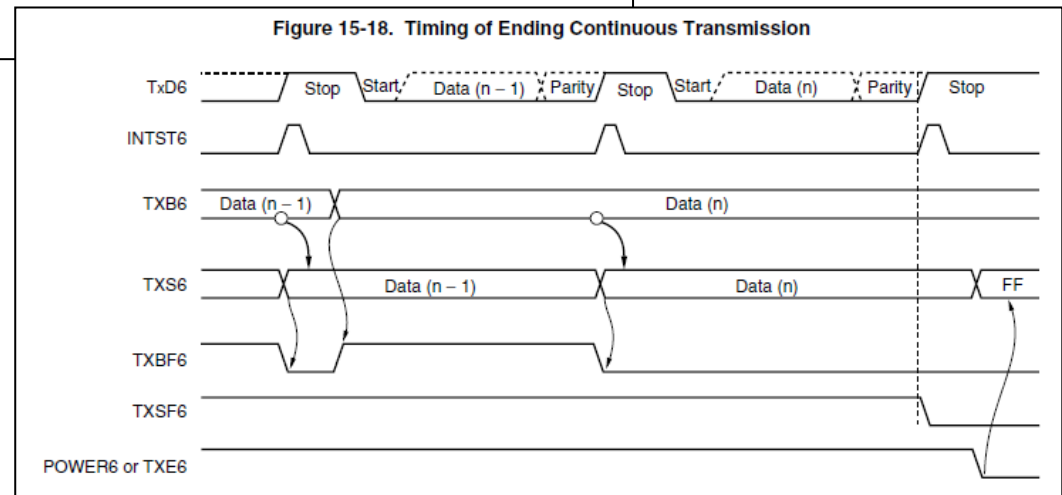


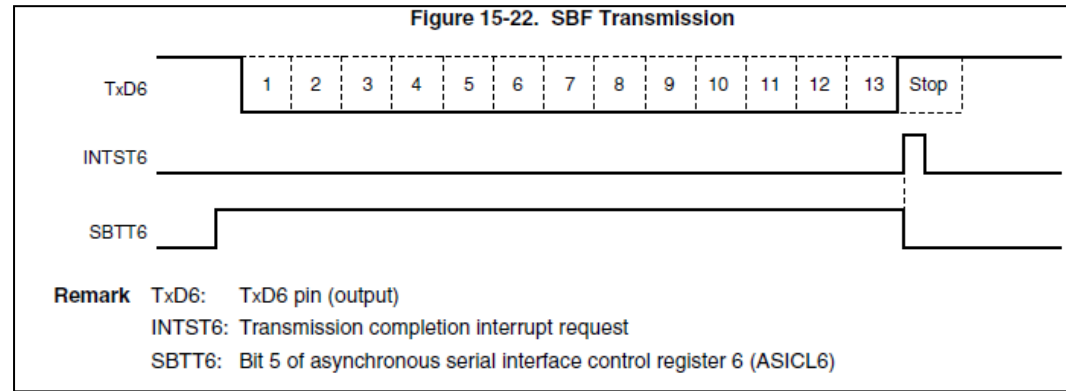
Figure 15-18. Timing of Ending Continuous Transmission



SBF operation for LIN-bus

▶ SBF transmission

- ▶ Started at SBTT6=1
- ▶ 전송 완료 후, 자동 클리어 SBT6=0



▶ SBF reception

