2011년2학기
임베디드시스템 응용(#514118)
#9. Serial communication 3
SPI, CSI10/11

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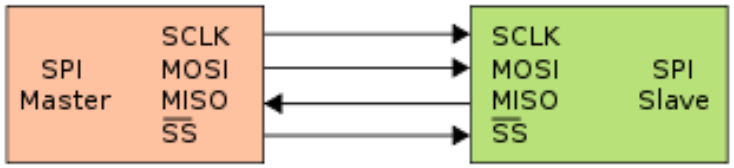
순 서

- SPI
  - Overview
  - Operation
- CSI10, CSI11
  - Configurations
  - Registers
  - Operations
  - Code

SPI

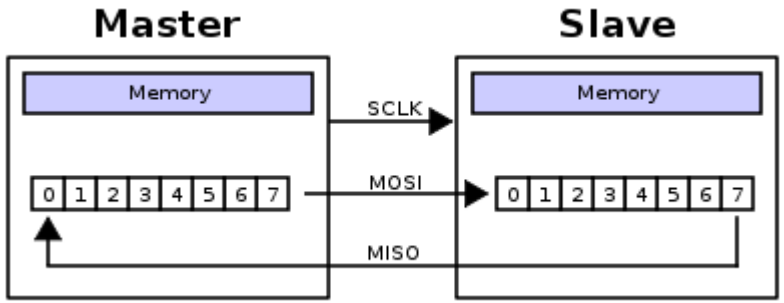
SPI

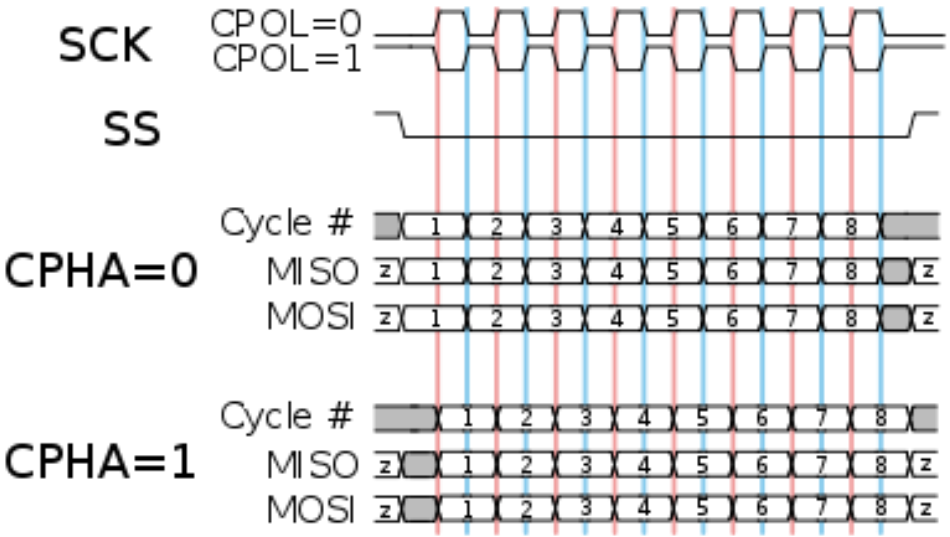
- Serial Peripheral Interface Bus
  - SPI bus
  - Synchronous serial data link
  - Made by Motorolla
  - Master/slave mode, multiple slave possible by slave select lines.
  - 4-wire serial bus ← 3, 2, 1-wire serial bus
- Interface
  - SCLK (SCK): serial clock
  - MOSI, SIMO: master output slave input, SDI:serial data in
  - MISO, SOMI: master input serial output, SDO
  - SS: slave select(active low), nCS; chip select



SPI Operation

- Single master w/ multiple slaves
- Data transmission
  - 클럭 설정 (1~70MHz) 후 통신을 원하는 slave장치 선택(SS(CS) low)
  - Full duplex 통신: 매 클럭마다 마스터는 MOSI라인으로 데이터 출력하면서 동시에 MISO라인으로 데이터 수신.
  - 대개 8bit data length
- Clock polarity
  - 클럭 주기 뿐만이 아니라 마스터는 클럭 극성도 설정해야 함.
  - CPOL=0: 클럭 신호의 기본 논리 값이 0(L), CPOL=1: H
  - CPHA=0: 첫번째 에지에서 샘플링, 1:두번째 에지에서 샘플링 의미
  - CPOL=0, CPHA=0 ➔ rising에서 데이터 캡쳐, falling에서 새로운 비트로 변경, CPHA=1이면?
  - CPOL=1, CPHA=0 ➔ falling에서 캡쳐, rising에서 변경.





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SPI 장점/단점

- 장점
  - Full duplex comm.
  - Higher throughput than I2C, SMBus
  - Complete protocol flexibility for the bits transferred
    - Not limited to 8-bit words
  - Extremely simple hardware interfacing
- 단점
  - Requires more pins than I2C
  - No in-band addressing; out-of-band chip select signals are required
  - No hardware flow control by the slave
  - No hardware slave acknowledgment
  - Support only one master device
  - No error checking protocol
  - Only handles short distances compared to RS-232, RS-485 or CAN-bus

3-wire serial bus
CSI10/11

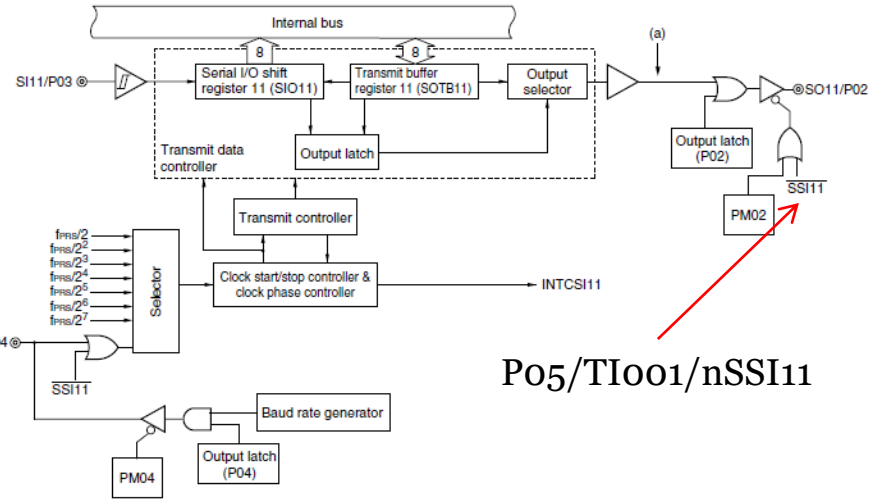
Configuration of CSI10/11

Table 16-1. Configuration of Serial Interfaces CSI10 and CSI11

Item	Configuration
Controller	Transmit controller Clock start/stop controller & clock phase controller
Registers	Transmit buffer register 1n (SOTB1n) Serial I/O shift register 1n (SIO1n)
Control registers	Serial operation mode register 1n (CSIM1n) Serial clock selection register 1n (CSIC1n) Port mode register 0 (PM0) or port mode register 1 (PM1) Port register 0 (P0) or port register 1 (P1)

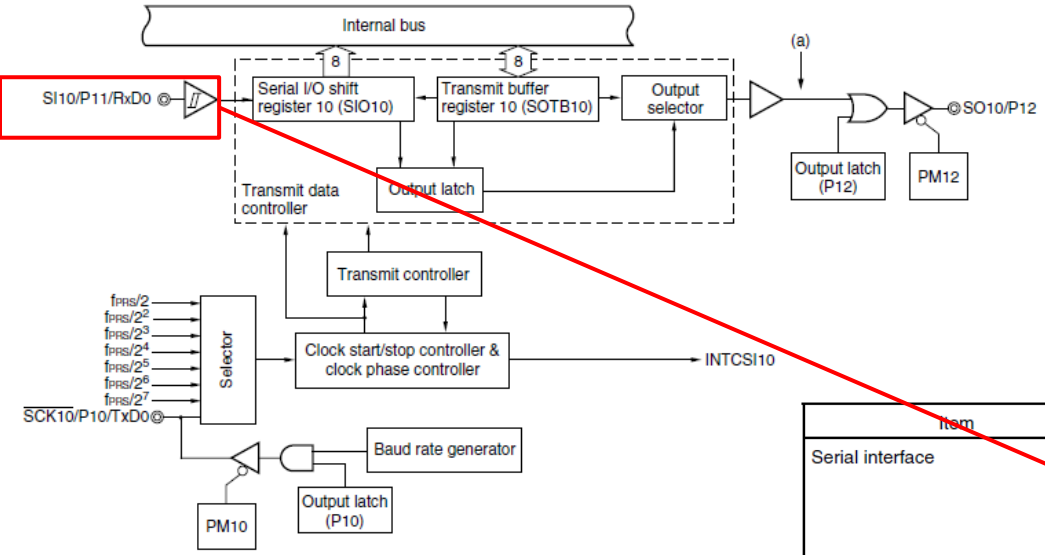
Remark n = 0, 1

Figure 16-2. Block Diagram of Serial Interface CSI11



P05/TI001/nSSI11

Figure 16-1. Block Diagram of Serial Interface CSI10



Item	μPD78F0544	μPD78F0545	μPD78F0546	μPD78F0547	μPD78F0547D
Serial interface	• UART supporting LIN-bus:			1 channel	
	• 3-wire serial I/O/UART[Note]:			1 channel	
	• 3-wire serial I/O:			1 channel	
	• 3-wire serial I/O with automatic transmit/receive function:			1 channel	
	• I^2C bus:			1 channel	

Remark (a): SO10 output

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Control registers

- CSIMIn (serial operation mode reg. In)

Figure 16-3. Format of Serial Operation Mode Register 10 (CSIM10)

Address: FF80H After reset: 00H R/W[Note 1]

Symbol	<7>	6	5	4	3	2	1	0
CSIM10	CSIE10	TRMD10	0	DIR10	0	0	0	CSOT10

CSIE10	Operation control in 3-wire serial I/O mode
0	Disables operation[Note 2] and asynchronously resets the internal circuit[Note 3].
1	Enables operation

TRMD10[Note 4]	Transmit/receive mode control
0[Note 5]	Receive mode (transmission disabled).
1	Transmit/receive mode

DIR10[Note 6]	First bit specification
0	MSB
1	LSB

CSOT10	Communication status flag
0	Communication is stopped.
1	Communication is in progress.

<7>	6	5	4	3	2	1	0
CSIE11	TRMD11	SSE11	DIR11	0	0	0	CSOT11

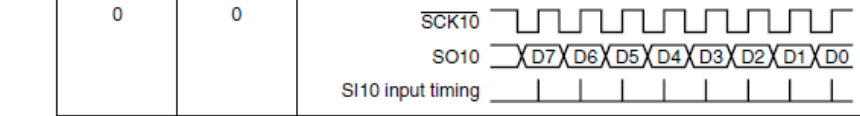
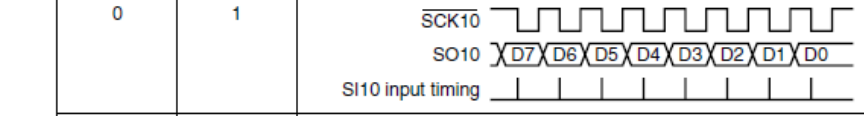
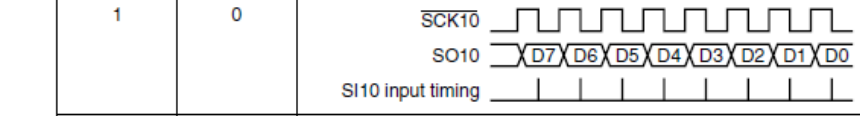
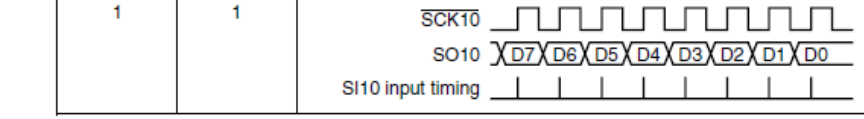
Control registers

- CSICIn
  - CKP=clock polarity (nSCK10 이므로 표준과 반대 동작)
    - CKP=0 → H, CKP=1 → L
  - DAP=nCPHA
    - DAP=1 → 1st edge operation, DAP=0 → 2nd edge
- Port setup
  - For output, PMx.x=0 Px.x=1
  - For input; PMx.x=1

Figure 16-5. Format of Serial Clock Selection Register 10 (CSIC10)

Address: FF81H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CSIC10	0	0	0	CKP10	DAP10	CKS102	CKS101	CKS100

CKP10	DAP10	Specification of data transmission/reception timing	Type
0	0		1
0	1		2
1	0		3
1	1		4

CKS102	CKS101	CKS100	CSI10 serial clock selection					Mode
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz	f_{PRS} = 20 MHz	
0	0	0	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	Master mode
0	0	1	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	
0	1	0	$f_{PRS}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	
0	1	1	$f_{PRS}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz	
1	0	0	$f_{PRS}/2^5$	62.5 kHz	156.25 kHz	312.5 kHz	625 kHz	
1	0	1	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz	312.5 kHz	
1	1	0	$f_{PRS}/2^7$	15.63 kHz	39.06 kHz	78.13 kHz	156.25 kHz	
1	1	1	External clock input to $\overline{SCK10}$					Slave mode

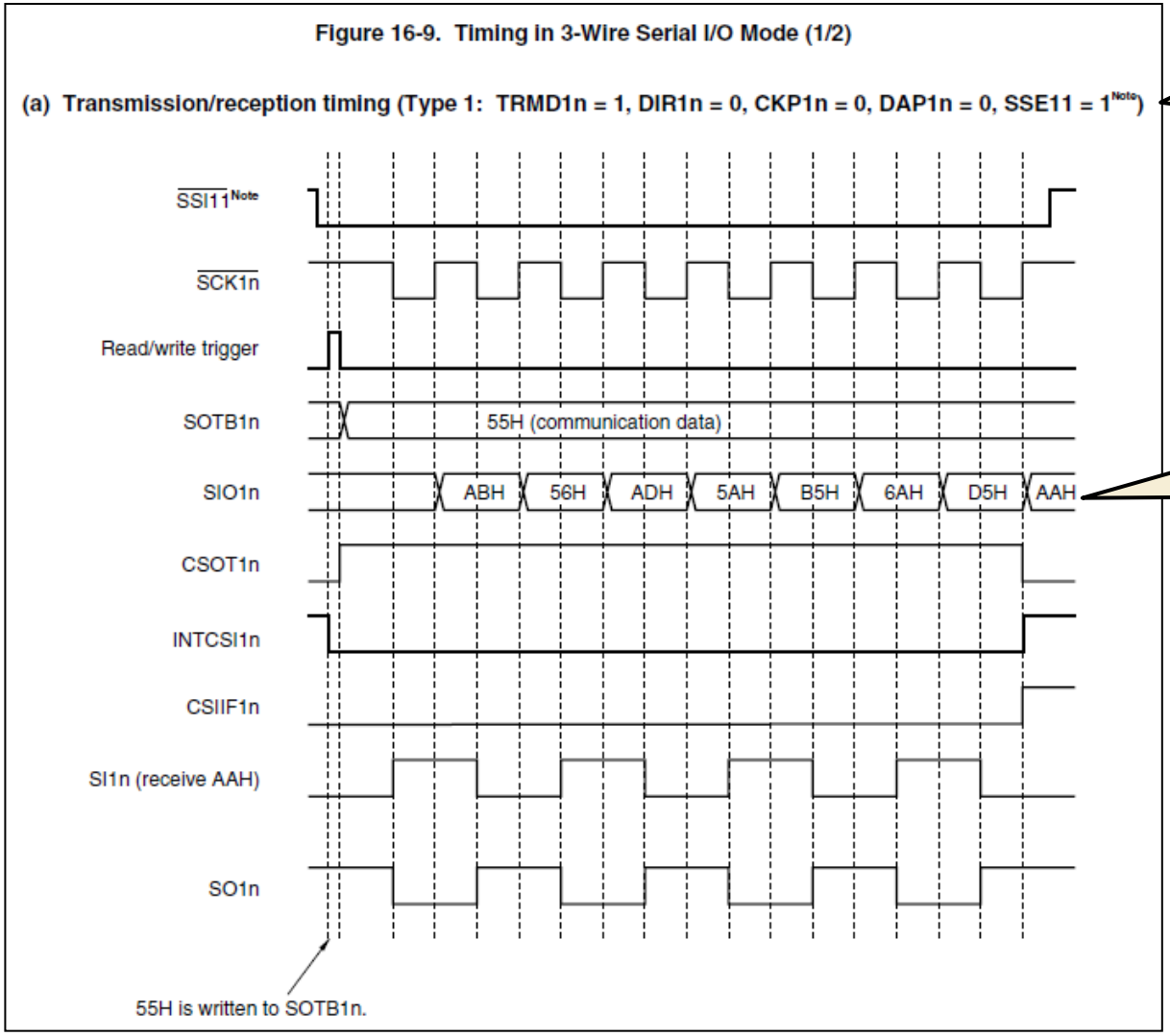
3-wire serial I/O operation

- Basic procedure
  - Set CSICln
  - Set DIRln, SSE, TRMDln of CSIMln
  - Set CSIEln =1
  - Write data to SOTBln → data transmission is started
    Read data from SIOln
- Register settings

(b) Serial interface CSI11

CSIE11	TRMD11	SSE11	PM03	P03	PM02	P02	PM04	P04	PM05	P05	CSI11 Operation	Pin Function			
												SI11/ P03	SO11/ P02	SCK11/ P04	SSI11/ TI001/P05
0	×	×	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	Stop	P03	P02	P04Note 2	TI001/ P05
1	0	0	1	×	×Note 1	×Note 1	1	×	×Note 1	×Note 1	Slave reception Note 3	SI11	P02	SCK11 (input) Note 3	TI001/ P05
		1							1	×					SSI11
1	1	0	×Note 1	×Note 1	0	0	1	×	×Note 1	×Note 1	Slave transmission Note 3	P03	SO11	SCK11 (input) Note 3	TI001/ P05
		1							1	×					SSI11
1	1	0	1	×	0	0	1	×	×Note 1	×Note 1	Slave transmission/ reception Note 3	SI11	SO11	SCK11 (input) Note 3	TI001/ P05
		1							1	×					SSI11
1	0	0	1	×	×Note 1	×Note 1	0	1	×Note 1	×Note 1	Master reception	SI11	P02	SCK11 (output)	TI001/ P05
1	1	0	×Note 1	×Note 1	0	0	0	1	×Note 1	×Note 1	Master transmission	P03	SO11	SCK11 (output)	TI001/ P05
1	1	0	1	×	0	0	0	1	×Note 1	×Note 1	Master transmission/ reception	SI11	SO11	SCK11 (output)	TI001/ P05

Operation: Timing



Clock polarity는 H, Phase는 2nd edge에서.

Lower bit부터 한 비트씩 입력되는 데이터로 변화되는 과정.

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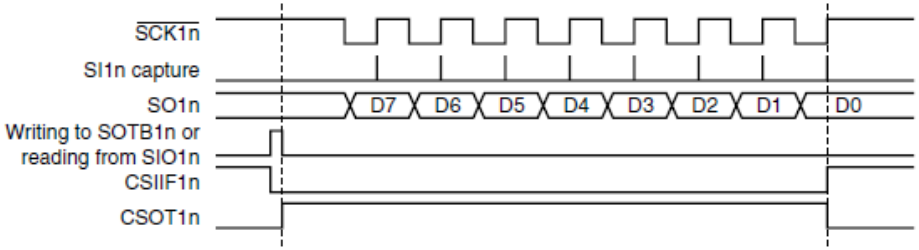
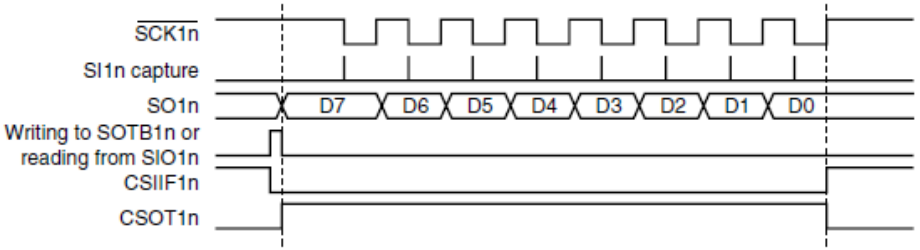
Clock/data phase timing for read

Figure 16-10. Timing of Clock/Data Phase

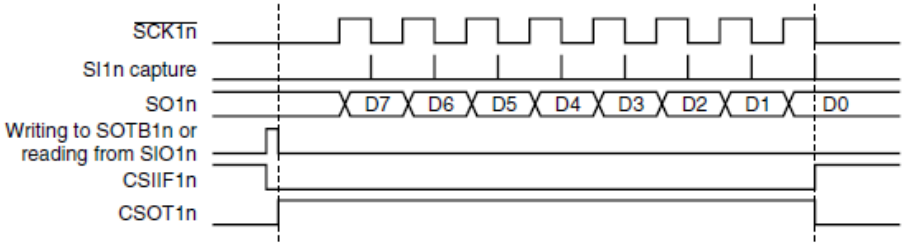
(a) Type 1: CKP1n = 0, DAP1n = 0, DIR1n = 0



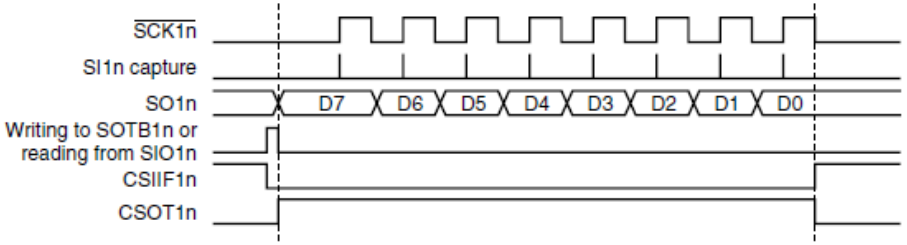
(b) Type 2: CKP1n = 0, DAP1n = 1, DIR1n = 0



(c) Type 3: CKP1n = 1, DAP1n = 0, DIR1n = 0



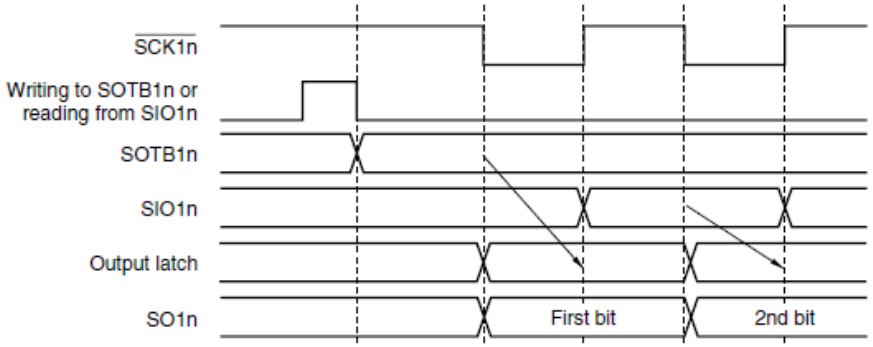
(d) Type 4: CKP1n = 1, DAP1n = 1, DIR1n = 0



Clock/data phase timing for writing

Figure 16-11. Output Operation of First Bit (1/2)

(a) Type 1: CKP1n = 0, DAP1n = 0



(b) Type 3: CKP1n = 1, DAP1n = 0

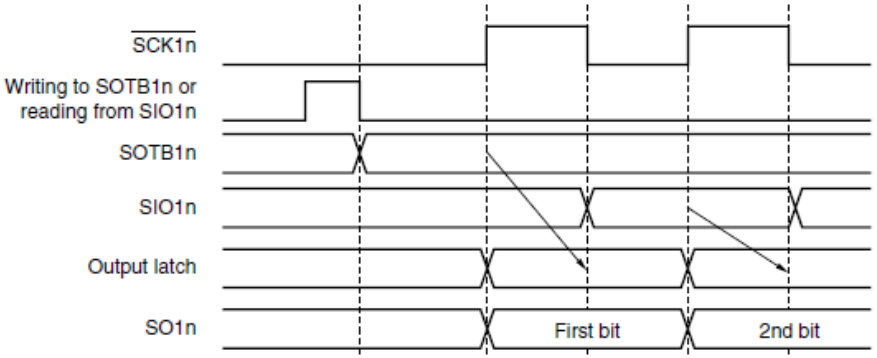


Figure 16-11. Output Operation of First Bit (2/2)

(c) Type 2: CKP1n = 0, DAP1n = 1

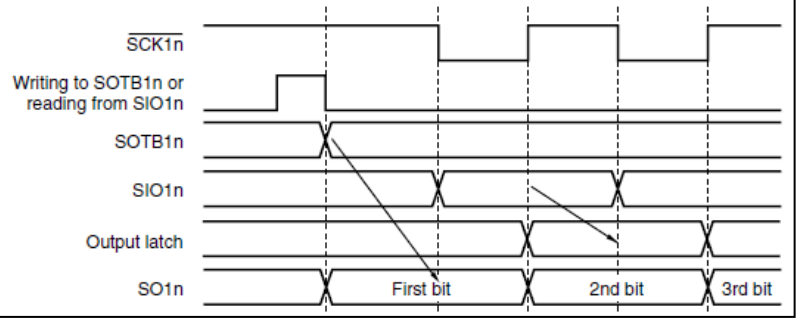
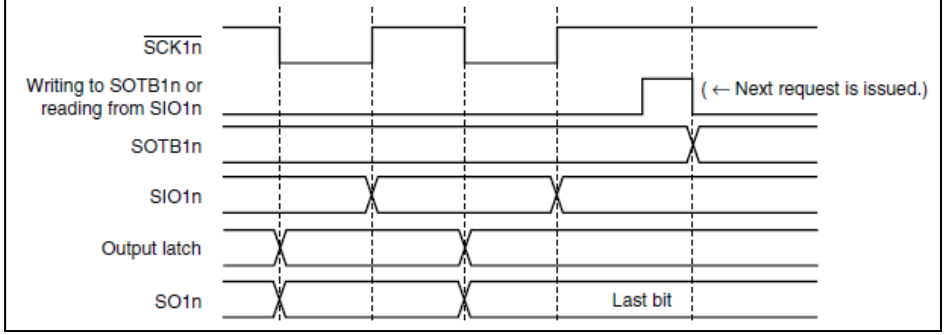


Figure 16-12. Output Value of SO1n Pin (Last Bit) (1/2)

(a) Type 1: CKP1n = 0, DAP1n = 0



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Code for CSI11

```
unsigned char data, rxflag;

#pragma vect INTCSI11 csi11_isr
__interrupt void csi11_isr(void)
{
        data = SIO11;
        rxflag = 1;
}
void main(void)
{
        //setup for CSI11
        CSIC11 = 0x03; //CKP=0, DAP=0, fclk=1.25MHz
        PM0 |= BIT4 + BIT2; P0 |= 0x14; //for output
        PM0.3 = 1; //for SI11
        CSIM11 = 0b11000000; //TRMD11=1, MSB first
        CSIMK11 = 0; //Irq. Mask flag for INTCSI11
        EI();
        while(1) {
           if(samp_flag)
              samp_flag=0,SOTB11 = 0x55; //send dumy data
           if(rxflag)
              rxflag=0; //process the received data..
        }
}
```

마스터인 장치가 슬레이브 장치로부터 센서 결과를 얻는 작업
*가정: 1:1로 연결, MSB first, Fclk=1.25MHz, No need /SS