2011년2학기
임베디드시스템 응용(#514118)
#10. Serial communication 4
I²C-bus, IIC0

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순 서

- I²C bus
  - Overview
  - Operation
- IIC0
  - Configurations
  - Registers
  - Operations
  - Code

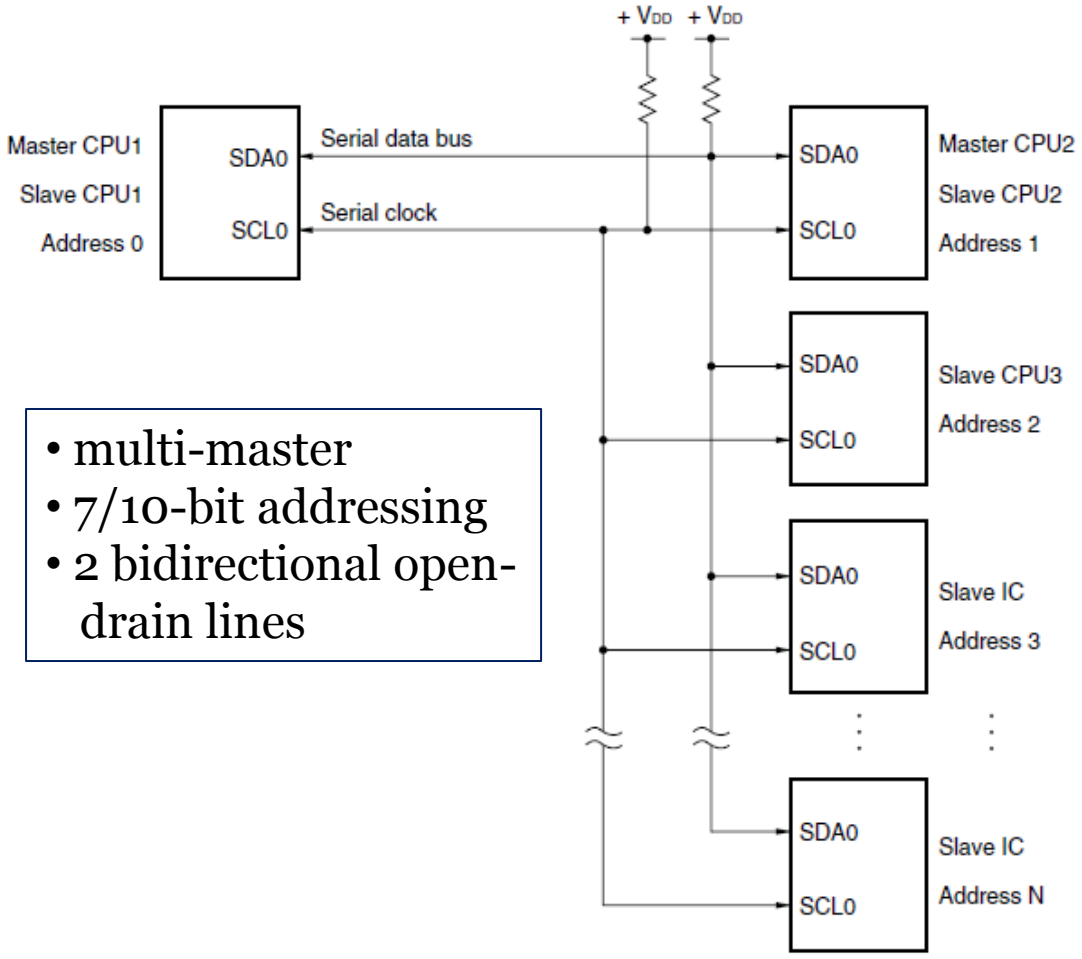
I^2C

I²C(Inter-Integrated Circuit) Bus

- Overview
  - i-two cee, i-squared cee, 2-wire interface
  - Multi-master serial single-ended computer bus
    - 7/10-bit address space
  - Philips 개발, 보급
  - 2006년 10월 이후 제조를 위한 licensing fee는 없어졌으나 slave address 획득을 위해서는 비용 필요.
  - 1995년 정의된 SMBus (System Management bus)는 I2C의 부분집합의 하나로 보다 엄격한 규칙 적용.
  - Spec. history
    - Version 1.0 – 1992: standard mode (~100kbps)/, fast mode(~400kbps)
    - V. 2.0- 1998: high-speed mode (Hs) (~3.4Mbps)
    - V. 2.1-2000
    - V. 3.0-2007: added Fast mode plus (Fm+)

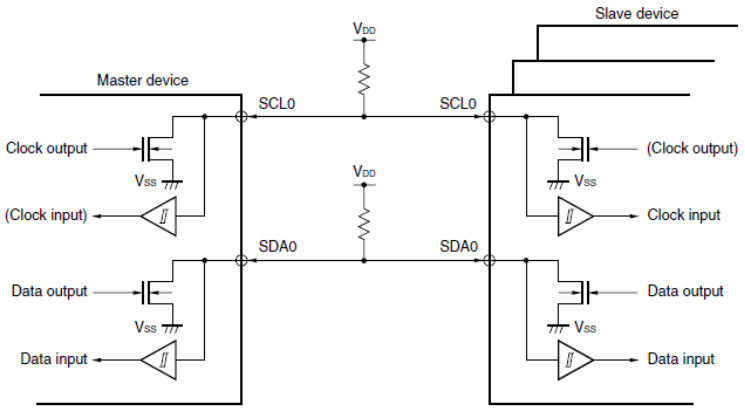
I2C bus connection

Figure 18-2. Serial Bus Configuration Example Using I²C Bus



- multi-master
- 7/10-bit addressing
- 2 bidirectional open-drain lines

Figure 18-11. Pin Configuration Diagram



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Operation of I2C

- Each node has 2 roles
  - Master node: issues the clock and address slaves.
  - Slave node: receives the clock line and address
- 4 Modes
  - Master transmit: sending data to a slave
  - Master receive: receiving data from a slave
  - Slave transmit: sending data to a master
  - Slave receive: receiving data from a master
- Starting/terminating
  - 마스터가 start bit(condition) 발생으로 시작, stop bit로 종료.

Figure 18-13. Start Conditions

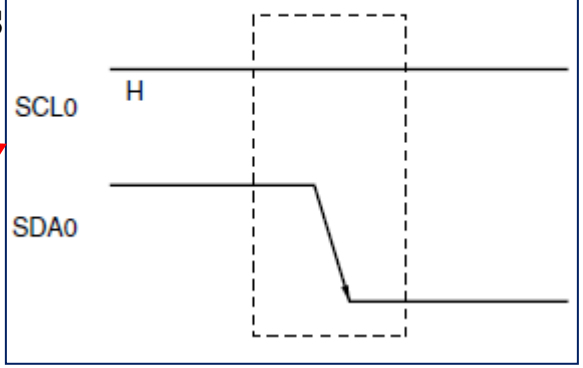


Figure 18-12. I²C Bus Serial Data Transfer Timing

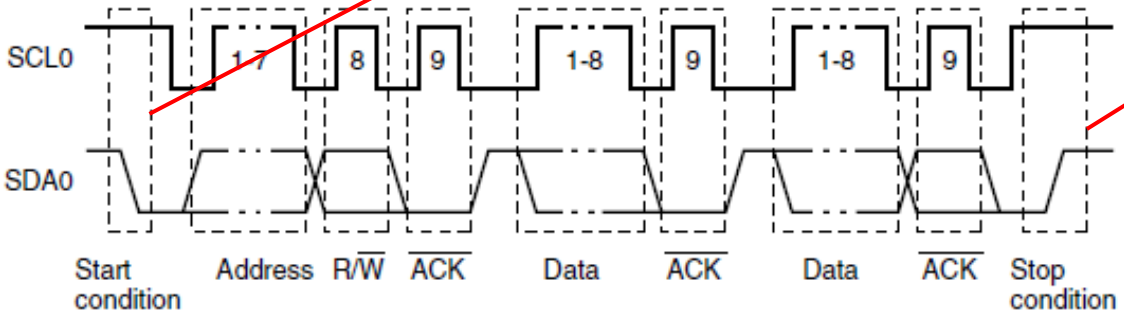
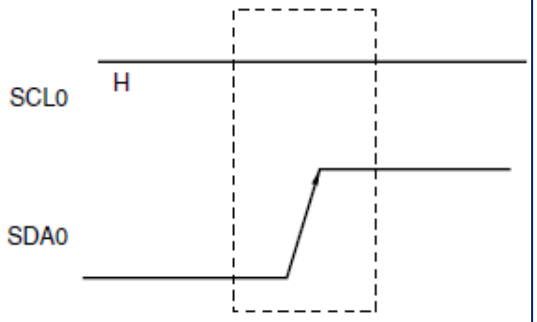


Figure 18-17. Stop Condition



Addressing I²C Devices

Figure A-2: 7-bit Address Format

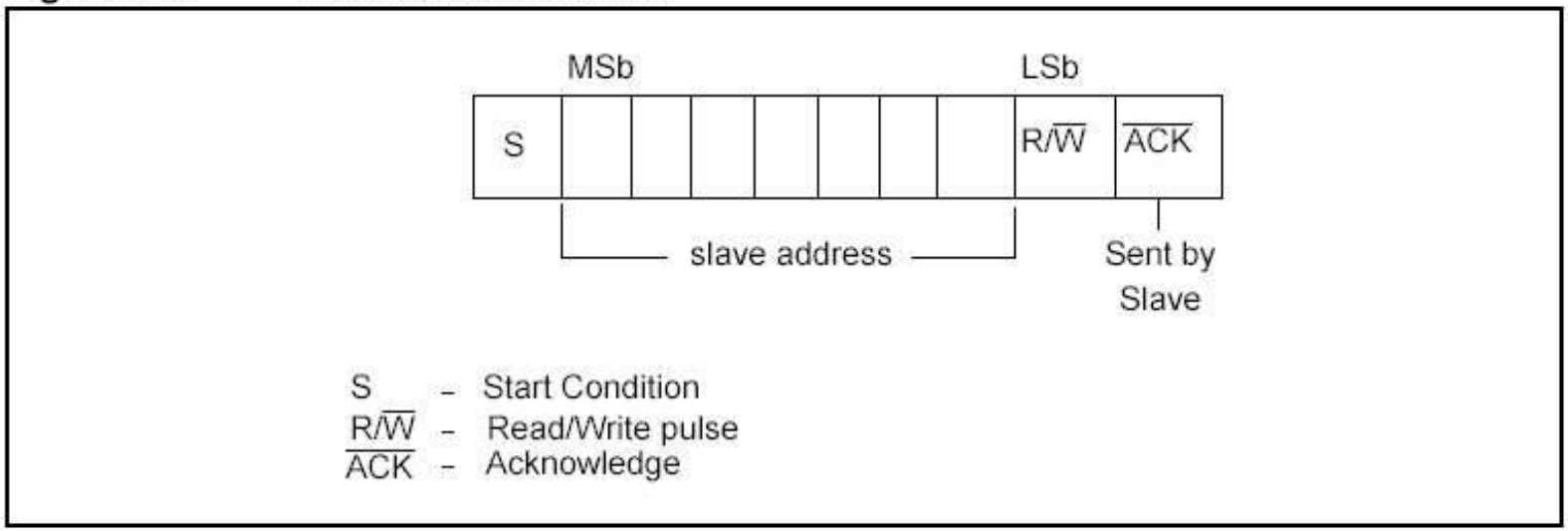
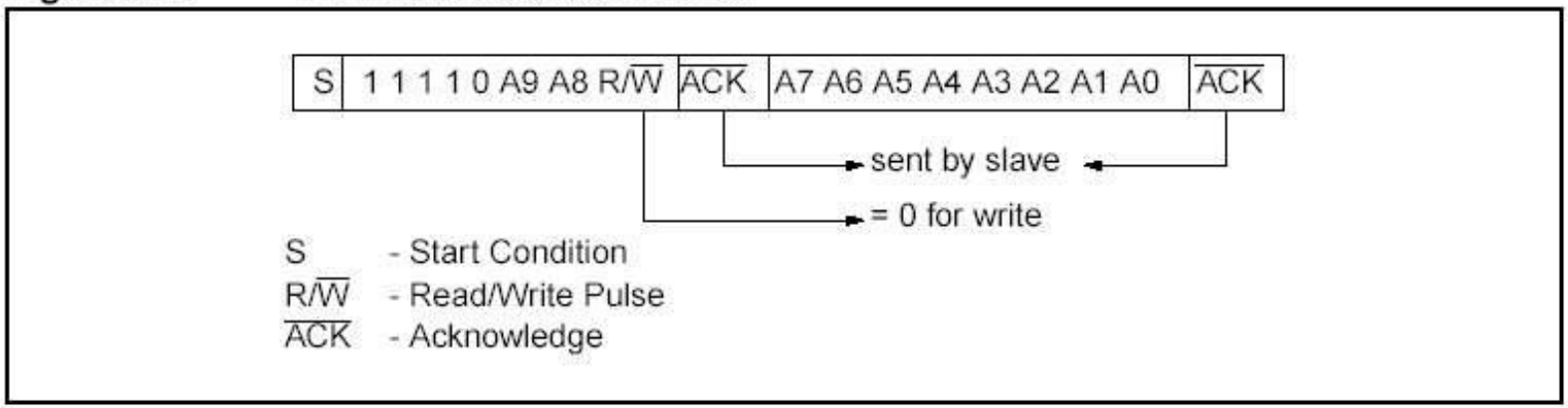
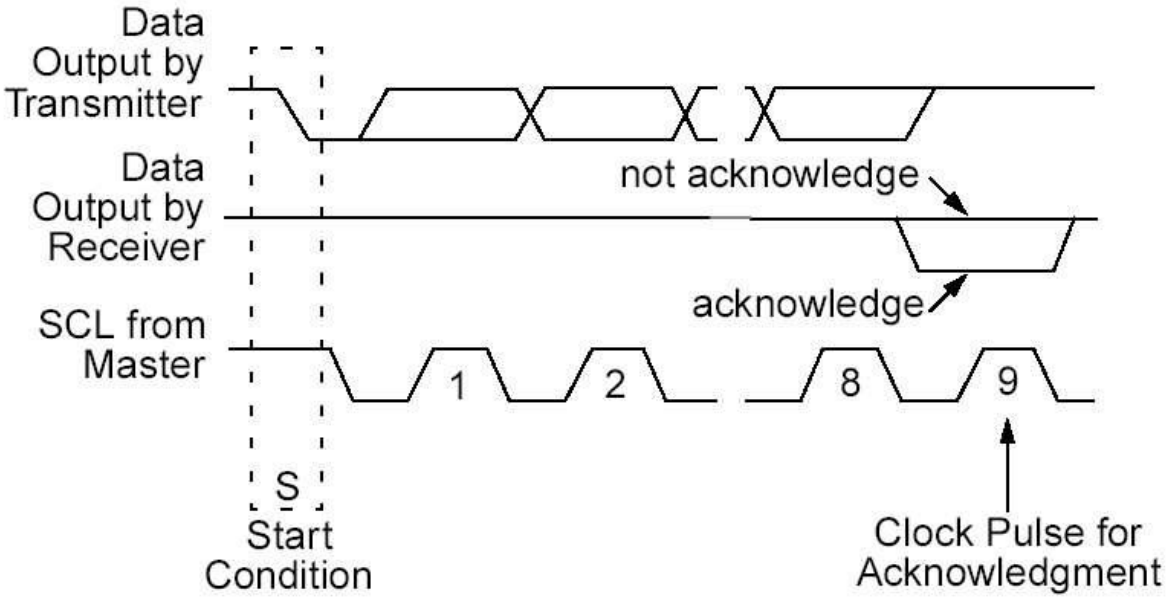


Figure A-3: I²C 10-bit Address Format



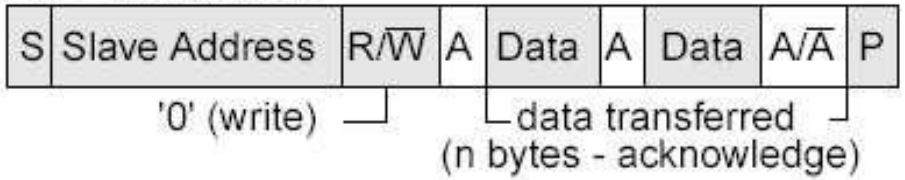
Transfer Acknowledge

- 모든 데이터는 바이트 단위로 전송되어야 함. 데이터의 개수의 제한은 없음.
- 각 바이트 전송 후에는 슬레이브(수신자)는 acknowledge bit (ACK)를 전송해야 함.
- 슬레이브가 ACK신호 보내지 않으면 마스터는 전송 중단.



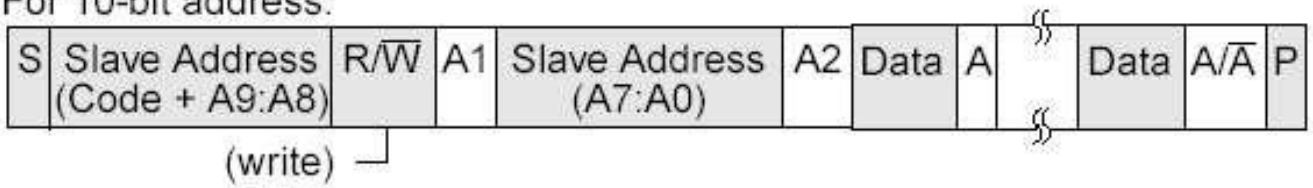
Master-Transmitter Sequence

For 7-bit address:



A master transmitter addresses a slave receiver with a 7-bit address. The transfer direction is not changed.

For 10-bit address:



A master transmitter addresses a slave receiver with a 10-bit address.

From master to slave

From slave to master

A = acknowledge (SDA low)
$\overline{A}$ = not acknowledge (SDA high)
S = Start Condition
P = Stop Condition

I^2C bus module
IIC0

Configuration of IIC0

Table 18-1. Configuration of Serial Interface IIC0

Item	Configuration
Registers	IIC shift register 0 (IIC0) Slave address register 0 (SVA0)
Control registers	IIC control register 0 (IICC0) IIC status register 0 (IICS0) IIC flag register 0 (IICF0) IIC clock selection register 0 (IICCL0) IIC function expansion register 0 (IICX0) Port mode register 6 (PM6) Port register 6 (P6)

7bit addressing support only.

Port seutp

- SCL0: P6.0
- SDA0: P6.1
- PM6.x=0
- P6.x=0

(Set IICE0=1 before port setup)

Control regs.: IICC0

- IIC control register 0 (IICC0)

Figure 18-5. Format of IIC Control Register 0 (IICC0) (1/4)

Address: FFA6H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICC0	IICE0	LREL0	WREL0	SPIE0	WTIM0	ACKE0	STT0	SPT0

- IICE0: en/disable module
- LREL0: 현재 통신 동작 취소하고 대기 상태로 만듬.
- WREL0: wait 취소
- SPIE0: Stop condition 발견 시 인터럽트 발생 유무 결정
- WTIM0: wait 시점 결정 (8/9번째 클럭)
- ACKE0: ACK 제어 (en/disable)
- STT0: Start condition trigger
- SPT0: Stop condition trigger

Control regs.: IICCL0

- IIC clock selection reg.0 (IICCL0)

Figure 18-8. Format of IIC Clock Selection Register 0 (IICCL0)

Address: FFA8H After reset: 00H R/W[Note]

Symbol	7	6	<5>	<4>	<3>	<2>	1	0
IICCL0	0	0	CLD0	DAD0	SMC0	DFC0	CL01	CL00

Read only

- SMC0: standard/high-speed mode 결정
  - Standard: 0~100KHz, high-speed:~400KHz
- DFC0: digital filter on/off in high-speed mode
- Clock speed selection:

Table 18-2. Selection Clock Setting

IICX0	IICCL0			Selection Clock (fw)	Transfer Clock (fw/m)	Settable Selection Clock (fw) Range	Operation Mode
Bit 0	Bit 3	Bit 1	Bit 0				
CLX0	SMC0	CL01	CL00				
0	0	0	0	$f_{PRS}/2$	fw/44	2.00 to 4.19 MHz	Normal mode (SMC0 bit = 0)
0	0	0	1	$f_{PRS}/2$	fw/86	4.19 to 8.38 MHz	
0	0	1	0	$f_{PRS}/4$	fw/86		
0	0	1	1	f_{EXSCL0}	fw/66	6.4 MHz	
0	1	0	×	$f_{PRS}/2$	fw/24	4.00 to 8.38 MHz	High-speed mode (SMC0 bit = 1)
0	1	1	0	$f_{PRS}/4$	fw/24		
0	1	1	1	f_{EXSCL0}	fw/18	6.4 MHz	
1	0	×	×	Setting prohibited			
1	1	0	×	$f_{PRS}/2$	fw/12	4.00 to 4.19 MHz	High-speed mode (SMC0 bit = 1)
1	1	1	0	$f_{PRS}/4$	fw/12		
1	1	1	1	Setting prohibited			

Control regs.: IICS0

- IIC status registers (IICS0)

Figure 18-6. Format of IIC Status Register 0 (IICS0) (1/3)

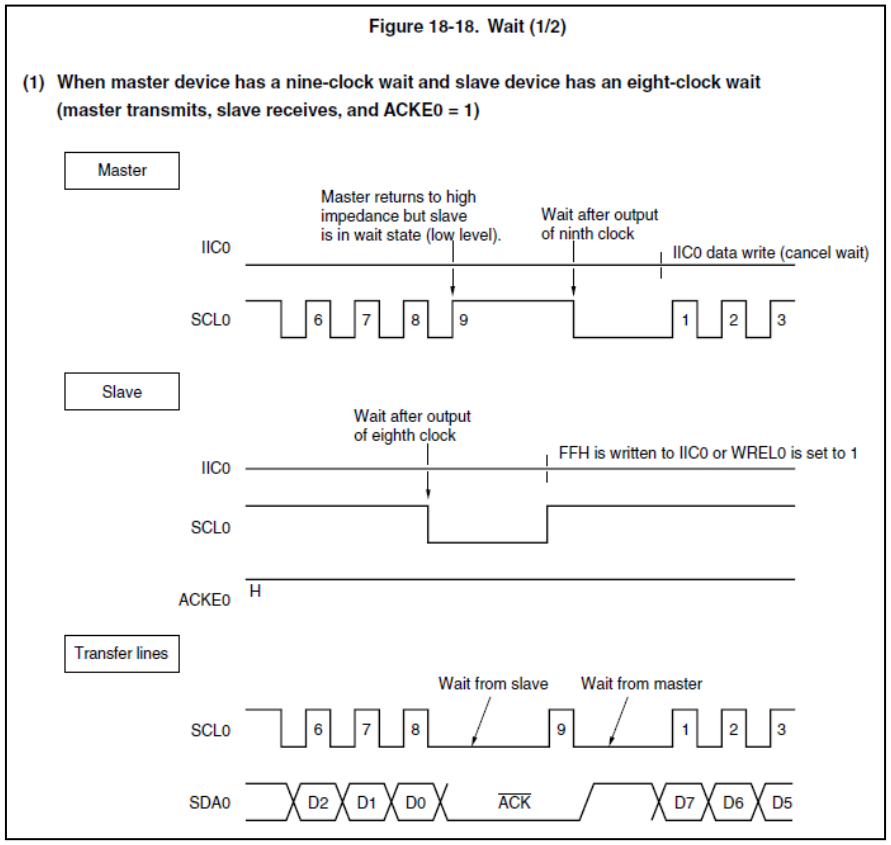
Address: FFAAH After reset: 00H R

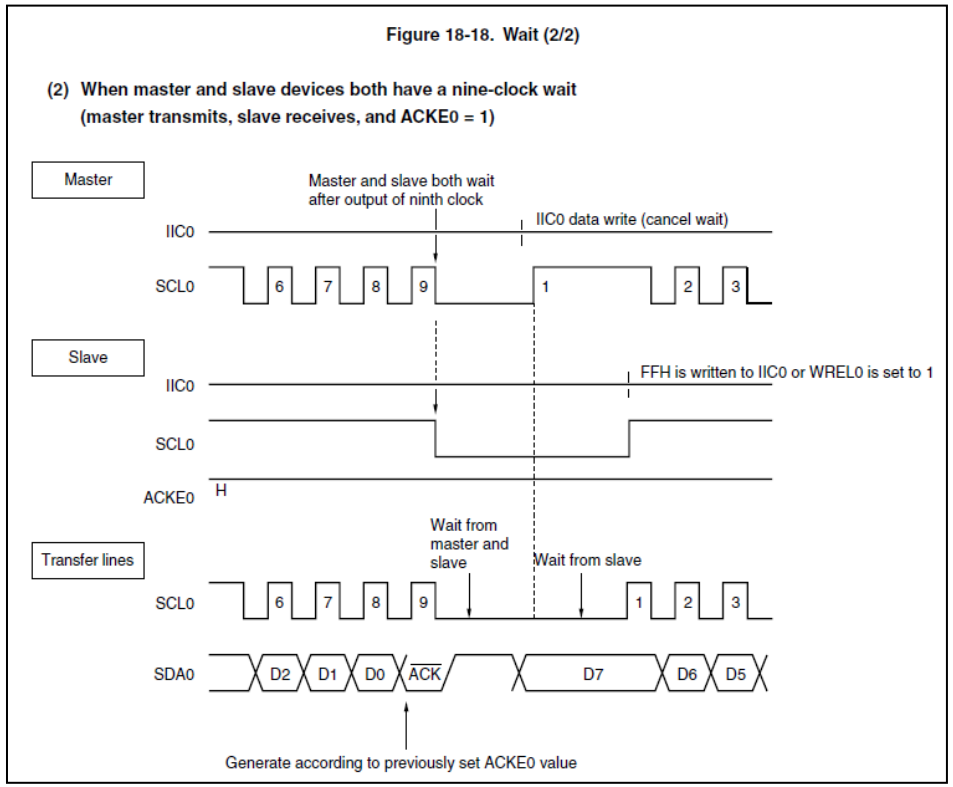
Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICS0	MSTS0	ALD0	EXC0	COI0	TRC0	ACKD0	STD0	SPD0

- MSTS0: master(1),slave/통신대기 상태(0)
- ALD0: arbitration loss, 1:loss, 0:win
- EXC0: detection of extension code (10bit add.)
- COI0: detection of matching add.
- TRC0: detection of tx/tx status, 0:rx, 1:tx
- ACKD0: detection of ack. (nACK)
- STD0: detection of start cond.
- SPD0: detection of stop cond.

Wait

- wait는 대화 상대에게 자신이 수/발신이 준비되었다는 것을 알리는 역할 (즉 wait state에 있음을 알림)





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Timing

- See Fig. 18-27~ 18-28